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## **BSS138**

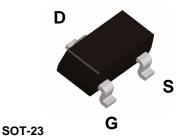
### N-Channel Logic Level Enhancement Mode Field Effect Transistor

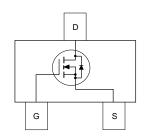
#### **General Description**

These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

#### **Features**

- 0.22 A, 50 V.  $R_{DS(ON)} = 3.5\Omega$  @  $V_{GS} = 10$  V  $R_{DS(ON)} = 6.0\Omega$  @  $V_{GS} = 4.5$  V
- High density cell design for extremely low R<sub>DS(ON)</sub>
- Rugged and Reliable
- Compact industry standard SOT-23 surface mount package





Absolute Maximum Ratings TA=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units	
V <sub>DSS</sub>	Drain-Source Voltage		50	V	
V <sub>GSS</sub>	Gate-Source Voltage		±20	V	
$I_D$	Drain Current - Continuous	(Note 1)	0.22	А	
	– Pulsed		0.88		
P <sub>D</sub>	Maximum Power Dissipation	(Note 1)	0.36	W	
	Derate Above 25°C		2.8	mW/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C	
TL	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds		300	°C	

#### **Thermal Characteristics**

R <sub>eJA</sub> Thermal Resistance, Junction-to-Ambient (No	1) 350	°C/W
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**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity	
SS	BSS138	7"	8mm	3000 units	

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = 250 \mu\text{A}$	50			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A,Referenced to 25°C		72		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 50 \text{ V}, \qquad V_{GS} = 0 \text{ V}$			0.5	μΑ
		$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V T}_{J} = 125^{\circ}\text{C}$			5	μΑ
		$V_{DS} = 30 \text{ V}, \qquad V_{GS} = 0 \text{ V}$			100	nA
I <sub>GSS</sub>	Gate-Body Leakage.	$V_{GS} = \pm 20 \text{ V},  V_{DS} = 0 \text{ V}$			±100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_{D} = 1 \text{ mA}$	0.8	1.3	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 1 mA,Referenced to 25°C		-2		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source	$V_{GS} = 10 \text{ V}, \qquad I_{D} = 0.22 \text{ A}$		0.7	3.5	Ω
	On–Resistance	$V_{GS} = 4.5 \text{ V}, \qquad I_D = 0.22 \text{ A}$		1.0	6.0	
I	On–State Drain Current	$V_{GS} = 10 \text{ V}, I_D = 0.22 \text{ A}, T_J = 125^{\circ}\text{C}$ $V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	0.2	1.1	5.8	A
I <sub>D(on)</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, \qquad V_{DS} = 3 \text{ V}$ $V_{DS} = 10 \text{ V}, \qquad I_{D} = 0.22 \text{ A}$	0.2	0.5		S
g <sub>FS</sub>		V <sub>DS</sub> = 10V, I <sub>D</sub> = 0.22 A	0.12	0.5		3
Dynamic C <sub>iss</sub>	Characteristics Input Capacitance	V 25 V V 0 V		27		pF
Coss	Output Capacitance	$V_{DS} = 25 \text{ V}, \qquad V_{GS} = 0 \text{ V},$ f = 1.0  MHz		13		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			6		pF
R <sub>G</sub>	Gate Resistance	V <sub>GS</sub> = 15 mV, f = 1.0 MHz		9		Ω
	g Characteristics (Note 2)	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, \qquad I_{D} = 0.29 \text{ A},$		2.5	5	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		9	18	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			20	36	ns
t <sub>f</sub>	Turn–Off Fall Time			7	14	ns
$\overline{Q_g}$	Total Gate Charge	$V_{DS} = 25 \text{ V}, \qquad I_{D} = 0.22 \text{ A},$		1.7	2.4	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		0.1		nC
Q <sub>gd</sub>	Gate-Drain Charge			0.4		nC
Drain-So	ource Diode Characteristics	and Maximum Ratings		•	· U	
I <sub>s</sub>	Maximum Continuous Drain–Source				0.22	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{S} = 0.44 \text{ A(Note 2)}$		0.8	1.4	V

#### Notes:

1.  $R_{\theta,JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta,JC}$  is guaranteed by design while  $R_{\theta,CA}$  is determined by the user's board design.



a) 350°C/W when mounted on a minimum pad..

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%

## **Typical Characteristics**

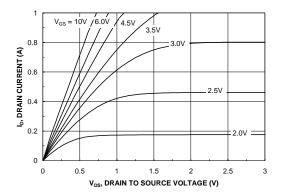


Figure 1. On-Region Characteristics.

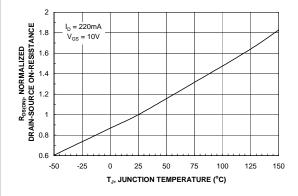


Figure 3. On-Resistance Variation with Temperature.

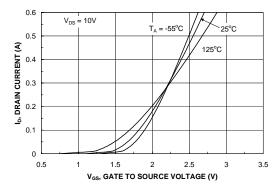


Figure 5. Transfer Characteristics.

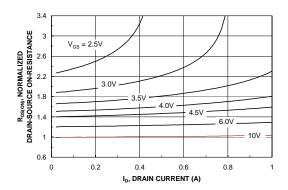


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

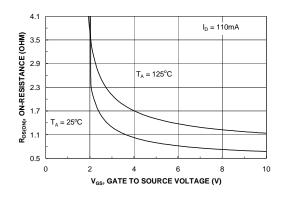


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

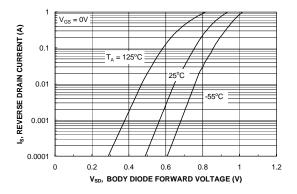
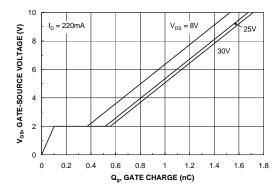


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## **Typical Characteristics**



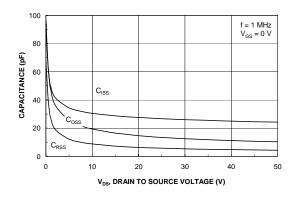


Figure 7. Gate Charge Characteristics.

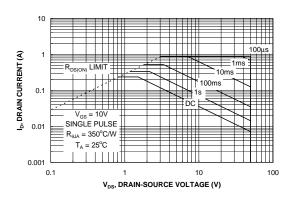


Figure 8. Capacitance Characteristics.

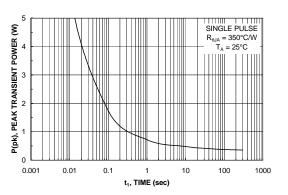


Figure 9. Maximum Safe Operating Area.



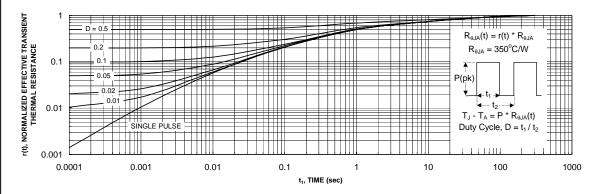


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1a. Transient thermal response will change depending on the circuit board design.



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