NCP1631PFCGEVB

Interleaved PFC Stage Driven by the NCP1631 Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Interleaved PFC is an emerging solution that becomes particularly popular in applications where a strict form factor has to be met like for instance, in slim notebook adapters or in LCD TVs. Interleaving consists in paralleling two "small" stages in lieu of a bigger one, which may be more difficult to design. Practically, two 150−W PFC stages are combined to form our 300−W PFC pre−regulator. This approach has several merits like the ease of implementation, the use of more but smaller components or a better heat distribution.

Also, Interleaving extends the power range of Critical Conduction Mode (CrM) that is an efficient and cost−effective technique (no need for low t_{rr} diodes). Even, as reported by NCP1631EVB/D [3], when associated to the **F**requency **C**lamped **Cr**itical conduction **M**ode (FCCrM), this technique yields particularly high efficiency levels (about 95% over a large load range at 90 V_{rms} in a 300−W application).

Furthermore, if the two stages are operated out−of−phase, the current ripple is significantly reduced. In particular, the input current looks like that of a Continuous Conduction Mode (CCM) one and the rms current within the bulk capacitor is dramatically reduced. These characteristics are detailed in application note AND8355 [1].

This paper gives the main equations that are useful to design an interleaved PFC stage driven by the NCP1631. The process is illustrated by the following 300−W, universal mains application:

Figure 1. Evaluation Board Photo

- Maximum output power: 300 W
- Input voltage range: from 90 V_{rms} to 265 V_{rms}
- Regulation output voltage: 390 V

The computations relevant to the power components are based on the assumption that the current is perfectly shared between the two branches. This assumption is valid if the two coil inductances properly match [2].

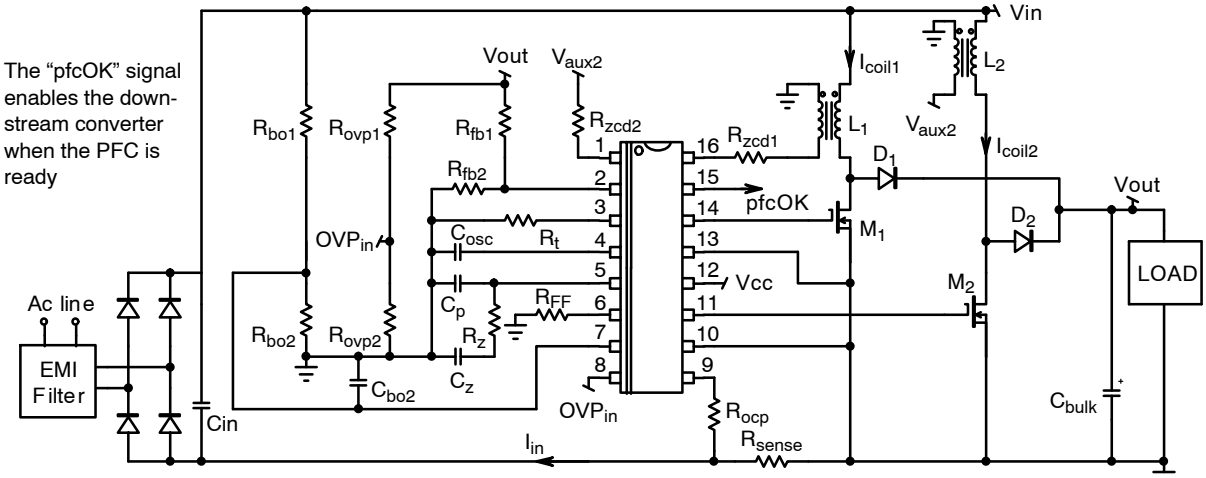


Figure 2. Generic Application Schematic

Introduction

The NCP1631 integrates a dual MOSFET driver for interleaved, 2−phase PFC applications. It drives the two branches in so−called ***F**requency **C**lamped **C**ritical conductio**n** **M**ode* (**FCCrM**) where each phase operates in ***C**ritical conduction **M**ode* (CrM) in the most stressful conditions and in ***D**iscontinuous **C**onduction **M**ode* (DCM) otherwise, acting as a CrM controller with a frequency clamp (given by the oscillator). According to the conditions, the PFC stage actually jumps from DCM to CrM (and vice versa) with no discontinuity in operation and without degradation of the current shape.

Furthermore, the circuit incorporates protection features for a rugged operation together with some special circuitry to lower the power consumed by the PFC stage in no−load conditions. More generally, the NCP1631 is ideal in systems where cost−effectiveness, reliability, low stand−by power and high power factor are the key parameters:

- **Fully Stable FCCrM and Out−Of−Phase Operation.**

Unlike master/slave controllers, the NCP1631 utilizes an interactive−phase approach where the two branches operate independently. Hence, the two phases necessarily operate in FCCrM, preventing risks of undesired dead−times or continuous conduction mode sequences. In addition, the circuit makes them interact so that they run out−of−phase. The NCP1631 unique interleaving technique substantially maintains the wished 180° phase shift between the 2 branches, in all conditions including start−up, fault or transient sequences.

- **Optimized Efficiency Over the Full Power Range.**

The NCP1631 optimizes the efficiency of your PFC stage in the whole line/load range. Its clamp frequency is a major contributor at nominal load. For medium and light load, the clamp frequency linearly decays as a function of the power to maintain high efficiency levels even in very light load. The power threshold under which frequency reduces is programmed by the resistor placed between pin 6 and ground. To prevent any risk of regulation loss at no load, the circuit further skips cycles when the error amplifier reaches its low clamp level.

- **Fast Line / Load Transient Compensation.**

Characterized by the low bandwidth of their regulation loop, PFC stages exhibit large over and under−shoots when abrupt load or line transients occur (e.g. at start−up). The NCP1631 dramatically narrows the output voltage range. First, the controller dedicates one pin to set an accurate Over−Voltage Protection level and interrupts the power delivery as long as the output voltage exceeds this threshold. Also, the NCP1631 ***dynamic response enhancer*** drastically speeds−up the regulation loop when the output voltage is 4.5% below its desired level. As a matter of fact, a PFC stage provides the downstream converter with a very narrow voltage range.

- **A “pfcOK” Signal.**

The circuit detects when the PFC stage is in steady state or if on the contrary, it is in a start−up or fault condition. In the first case, the “pfcOK” pin (pin15) is in high state and low otherwise. This signal is to disable the downstream converter unless the bulk capacitor is charged and no fault is detected. Finally, the downstream converter can be optimally designed for the narrow voltage provided by the PFC stage in normal operation.

- **Safety Protections.**

The NCP1631 permanently monitors the input and output voltages, the input current and the die temperature to protect the system from possible over−stresses and make the PFC stage extremely robust and reliable. In addition to the aforementioned OVP protection, one can list:

Maximum Current Limit: the circuit permanently senses the total input current and prevents it from exceeding the preset current limit, still maintaining the out−of−phase operation.

In−rush Detection: the NCP1631 prevents the power switches turn on for the large in−rush currents sequence that occurs during the start−up phase.

Under−Voltage Protection: this feature is mainly to prevent operation in case of a failure in the OVP monitoring network (e.g., bad connection).

Brown−Out Detection: the circuit stops operating if the line magnitude is too low to protect the PFC stage from the excessive stress that could damage it in such conditions.

Thermal Shutdown: the circuit stops pulsing when its junction temperature exceeds 150°C typically and resumes operation once it drops below about 100°C (50°C hysteresis).

Power Components

Defining the oscillator frequency of the NCP1631 is a prerequisite step before dimensioning the PFC stage. In the presented application, we choose to clamp the switching frequency at around 120 kHz in each phase, because this frequency is generally a good trade−off when considering the following aspects:

- A high switching frequency reduces the size of the storage elements. In particular, it is well known that the higher the switching frequency, the lower the inductor core. That is why, one should set the switching frequency as high as possible,
- On the other hand, increasing the switching frequency has two major drawbacks:
  1. The switching rate increasing, the associated losses grow up. In addition, all parasitic capacitors charge at a higher frequency and generate more heat...
  2. EMI filtering is tougher: the switching generates high EMI rays at the switching frequency and

close harmonic levels. Most power supplies have to meet the CISPR22 standard that applies to frequencies above 150 kHz. That is why SMPS designers often select F_{SW} = 130 kHz so that the fundamental keeps below 150 kHz and then out of the regulation scope. Often, 65 kHz is also chosen to not to have to damp harmonic 2 too.

The oscillator frequency is the double of the clamp frequency in each phase. The oscillator frequency is then set to approximately 240 kHz .

Basically, Two 150−W FCCrM PFC stages are to be designed. This chapter will not detail the dimensioning of the power components in very deep details since their computation is traditional. However, the main selection criteria and equations are reminded.

1. Inductor Selection

In CrM and in FCCrM (assuming CrM operation at low line, full load), the (maximum) peak and rms inductor currents within one branch are:

$$\left(I_{L(pk)}\right)_{MAX} = \frac{2\sqrt{2}\cdot\left(\frac{(P_{in,avg})_{max}}{2}\right)}{\left(V_{in(rms)}\right)_{LL}} = \frac{\sqrt{2}\cdot 325}{90} \cong 5.1\ A \quad \text{(eq. 1)}$$

And:

$$\left(I_{L(rms)}\right)_{MAX} = \frac{\left(I_{L(pk)}\right)_{MAX}}{\sqrt{6}} \cong \frac{5.1}{\sqrt{6}} = 2.1\ A \quad \text{(eq. 2)}$$

Where:

- $(V_{in,rms})_{LL}$ is the lowest line rms voltage
- $(P_{in,avg})_{max}$ is the maximum level of the input average power
- $V_{out,nom}$ is the nominal output voltage (regulation level)

In our application,

- $(V_{in,rms})_{LL}$ = 90 V
- $V_{out,nom}$ = 390 V
- $(P_{in,avg})_{max}$ = 325 W (assuming a 92 % global efficiency that is a conservative value that offers some margin)

As aforementioned, the frequency clamp for the two branches is set to about 120 kHz. The inductor must be large enough so that Critical conduction Mode is obtained at low line, full load where the conditions are the most severe.

This constraint leads to the equation below (where $f_{sw(max)}$ is the 120−kHz clamp frequency):

$$L \geq \frac{(V_{in,rms})_{LL}^{\ 2}\cdot(V_{out}-\sqrt{2}\cdot(V_{in,rms})_{LL})}{(P_{in,avg})_{max}\cdot V_{out,nom}\cdot f_{sw(max)}} \quad \text{(eq. 3)}$$

In our application, this leads to:

$$L \geq \frac{90^2\cdot\left(390-(\sqrt{2}\cdot 90)\right)}{325\cdot 390\cdot 120\cdot 10^3} \cong 139\ \mu H \quad \text{(eq. 4)}$$

Finally, a 150 µH / 6 A_{pk} / 2.5 A_{rms} coil was selected.

2. Power Semiconductors

The bridge diode should be selected based on the peak current rating and the power dissipation given by:

$$P_{bridge} = \frac{4\sqrt{2}}{\pi}\cdot V_f\cdot\frac{(P_{in,avg})_{max}}{(V_{in(rms)})_{LL}} \cong 1.8\cdot V_f\cdot\frac{325}{90} \cong 6.5\cdot V_f \quad \text{(eq. 5)}$$

Assuming a 1−V forward voltage per diode (V_f = 1 V), the bridge approximately dissipates 6.5 W.

For each branch, the MOSFET is selected based on the peak voltage stress ($V_{out(max)}$+margin) and on the rms current flowing through it ($I_{M(rms)}$):

$$I_{M(rms)} = \frac{2}{\sqrt{3}}\cdot\frac{\left(\frac{(P_{in,avg})_{max}}{2}\right)}{(V_{in(rms)})_{LL}}\cdot\sqrt{1-\frac{8\cdot\sqrt{2}\cdot(V_{in(rms)})_{LL}}{3\cdot\pi\cdot V_{out,nom}}} = \frac{325}{\sqrt{3}\cdot 90}\cdot\sqrt{1-\frac{8\cdot\sqrt{2}\cdot 90}{3\cdot\pi\cdot 390}} \cong 1.8\ A \quad \text{(eq. 6)}$$

Using a 600−V, 0.4−Ω FET (SPP11N60), will give conduction losses of (assuming that $R_{DS(on)}$ increases by 80% due to temperature effects):

$$P_{cond} = I_{M(rms)}^{\ 2}\cdot R_{DS(on)} = 1.8^2\cdot 0.4\cdot 1.8 \cong 2.3\ W \quad \text{(eq. 7)}$$

This computation is valid for one branch. As there are two phases to consider, the total MOSFETs conduction losses are actually twice (4.6 W).

Switching losses are hard to predict. They are not computed here. As a rule of the thumb, we generally reserve a loss budget equal to that of the conduction ones. One can anyway note that the NCP1631 limits this source of dissipation by clamping the switching frequency (that can never exceed the oscillator one – 120 kHz in each branch in our case). To further improve the efficiency, the MOSFET opening can be accelerated using the schematic of Figure 3, where the Q_1 small npn transistor (TO92) amplifies the MOSFET turn off gate current.

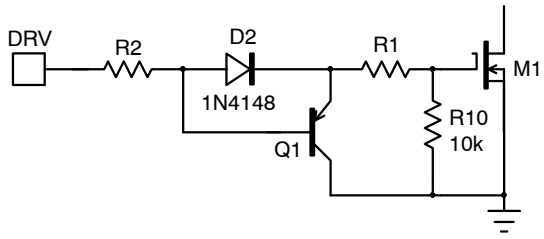


Figure 3. Q1 Speeds Up the MOSFET Turn Off

The input bridge that rectifies the line voltage and the MOSFETs of the two branches share the same heat−sink. Based on above computations, the total power to be dissipated is in the range of: (6.5 + 4.6 + 4.6 ≅ 16 W). A 2.9−°C/W heat−sink (ref. 437479 from AAVID THERMALLOY) is implemented. It limits the rise of the case temperature (of the input bridge and MOSFETs applied to it) to about 50° compared to the ambient temperature.

Interleaved PFC requires two boost diodes (one per branch). No reverse recovery issues to worry about. Simply, they must meet the correct voltage rating ($V_{out(max)}$ + margin) and exhibit a low forward voltage drop. Supposing a perfect current sharing, the average diode current is the half of the load one:

$$\left(I_{D1(avg)} = I_{D2(avg)} = \frac{I_{D(tot)_{(avg)}}}{2} = \frac{I_{LOAD}}{2} = \frac{P_{out}}{2 \cdot V_{out}} \cong 0.39\ A\right)$$

So, the losses are about

$$\left(\frac{I_{LOAD} \cdot V_f}{2}\right)$$

per diode, i.e., less than 500 mW per diode using MUR550 rectifiers. For each phase, the peak current seen by the diode will be the same as the corresponding inductor peak current. Two axial MUR550 are selected.

3. Bulk Capacitor Design

The output capacitor is generally designed considering three factors:

1. The maximum permissible low frequency ripple of the output voltage. The input current and voltage being both sinusoidal, PFC stages deliver a squared sinusoidal power that matches the load power demand in average only. As a consequence, the output voltage exhibits a low frequency ripple (e.g., 100 Hz ripple in Europe or 120 Hz in USA) that is inherent to the PFC function.
2. The rms magnitude of the current flowing through the bulk capacitor. Based on this computation, one must estimate the maximal permissible ESR not to cause an excessive heating.
3. The hold−up time. It can be specified that the power supply must provide the full power for a short mains interruption that is the so called hold−up time. The hold−up time is generally in the range of 10 or 20 ms.

The output voltage ripple is given by:

$$\Delta V_{out(p-p)} = \frac{P_{out}}{2\pi \cdot f_{line} \cdot C_{bulk} \cdot V_{out,nom}} \quad \text{(eq. 8)}$$

The capacitor rms current is given by (assuming a resistive load):

$$I_{C(rms)} = \sqrt{\frac{16 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot (V_{in(rms)})_{LL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out,nom}}\right)^2} \quad \text{(eq. 9)}$$

Finally the following equation expresses the hold−up time:

$$t_{hold-up} = \frac{C_{bulk} \cdot (V_{out}^2 - V_{out(min)}^2)}{2 \cdot P_{out}} \quad \text{(eq. 10)}$$

Where $V_{out(min)}$ is the minimal bulk voltage necessary to the downstream converter to keep properly feeding the load.

The hold−time being not considered here, a 100−μF capacitor was chosen to satisfy the other above conditions. The peak−peak ripple is 25 V (±3% of V_{out}) and the rms current is 1.4 A.

Oscillator Frequency Setting

The NCP1631 clamps the maximum frequency of the PFC stage without power factor degradation. This feature prevents the switching frequency from reaching excessive levels at light load. As detailed in the NCP1631 data sheet, the clamp frequency in each phase is actually half the oscillator one.

Hence:

$$f_{sw(max)1} = f_{sw(max)2} = f_{sw(max)} = \frac{f_{OSC}}{2} \quad \text{(eq. 11)}$$

Where:

- $f_{sw(max)1}$ is the frequency clamp for the first branch of the interleaved PFC and $f_{sw(max)2}$, that of the second one
- $f$sw(max)1 and $f$sw(max)2 being equal, $f$sw(max) stands for the clamp frequency for any of the two phases
- f_{OSC} is the oscillator frequency

In the absence of frequency foldback (heavy load in general), the oscillator swings at its nominal frequency $f_{OSC(nom)}$ and each branch operates with a nominal clamp frequency $(f_{sw(max)})_{nom}$ given by:

$$(f_{sw(max)})_{nom} = \frac{f_{OSC(nom)}}{2} \cong \frac{26 \cdot 10^{-6}}{C_{pin4}} \quad \text{(eq. 12)}$$

For instance, a 220−pF capacitor leads to the following clamp frequency:

$$(f_{sw(max)})_{nom} \cong \frac{26 \cdot 10^{-6}}{220 \cdot 10^{-9}} \cong 118\ kHz \quad \text{(eq. 13)}$$

Frequency Fold−back:

The NCP1631 features the frequency fold−back function to improve the light load efficiency. Practically, the oscillator charge and discharge currents are not constant but proportional to power when the load drops below a programmable level, as shown by Figure 4.

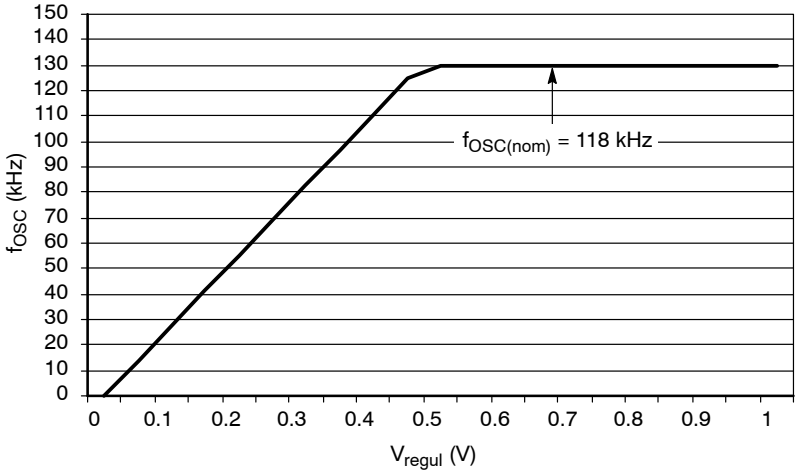


Figure 4. Frequency Fold−back

• Programming the Power Threshold for Frequency Foldback:

Pin6 of the NCP1631 pins out the signal V_{REGUL} that is proportional to the power that is delivered. The resistor (R_{FF}) placed between pin 6 and ground, adjusts the pin6 current (I_{FF}) as follows:

$$I_{FF} = \frac{V_{REGUL}}{R_{FF}} \qquad \text{If } \left(\frac{V_{REGUL}}{R_{FF}} \leq 105\ \mu A\right)$$

$$I_{FF} = 105\ \mu A \text{ otherwise}$$

As a matter of fact, the clamp frequency is also an increasing function of V_{REGUL} until it reaches a maximum value for (I_{OSC} = 105 μA):

$$f_{OSC} = f_{OSC(nom)} \qquad \text{If } \left(V_{REGUL} \geq R_{FF} \cdot 105\ \mu A\right)$$

$$f_{OSC} = \frac{V_{REGUL}}{R_{FF} \cdot 105\ \mu} \cdot f_{OSC(nom)} \qquad \text{If } \left(V_{REGUL} \leq R_{FF} \cdot 105\ \mu A\right)$$

V_{REGUL} varies between 0 and 1.66 V. Since the power that can be delivered is proportional to V_{REGUL}, the power threshold for frequency fold−back is:

$$(P_{in})_{FF} = \frac{R_{FF} \cdot 105\ \mu A}{1.66\ V} \cdot (P_{in})_{HL} \cong \frac{R_{FF}}{15810} \cdot (P_{in})_{HL} \quad \text{(eq. 14)}$$

Where:

- $(P_{in})_{FF}$ is the input power below which the frequency reduces
- $(P_{in})_{HL}$ is the power highest level that can virtually be delivered by the PFC stage. This value results from the timing resistor selection (see the “maximum power adjustment” section) and is generally set 25% or 30% higher than the application maximum power to offer some margin.

In our application, a 4.7−kΩ resistor is implemented on pin 6 (R_{FF} = 4.7 kΩ). Hence, the frequency folds back when the input power drops below the following $(P_{in})_{FF}$ threshold:

$$(P_{in})_{FF} = \frac{4.7 \cdot 10^3}{15810} \cdot (P_{in})_{HL} \cong 30\% \cdot (P_{in})_{HL} \quad \text{(eq. 15)}$$

In our application, the maximum input power is 325 W. It is recommended to design the PFC stage so that it can produce at least 25% more than the maximum power it targets. In practice, ($(P_{in})_{HL} \cong$ 494 W) has been selected. As a matter of fact, the frequency folds back when the input power goes below (30% x $(P_{in})_{HL}$) that is about 147 W.

• Forcing a Minimum Frequency

The NCP1631 reduces the frequency down to virtually zero. As detailed in the data sheet and shown by the simplified oscillator representation of Figure 5, the circuit lowers the frequency by diminishing the I_{FF} current. When this current is near zero, a 35−μA current source is still available for charging the oscillator capacitor but the discharge current is near zero leading to an extremely long discharge time and a very low frequency.

It is wise to prevent the frequency from dropping below 16 kHz to avoid audible noise issues. A simple means consists of placing a resistor (R_{Fmin}) between the “OSC” pin and ground to force a minimum oscillator discharge current (see Figure 5).

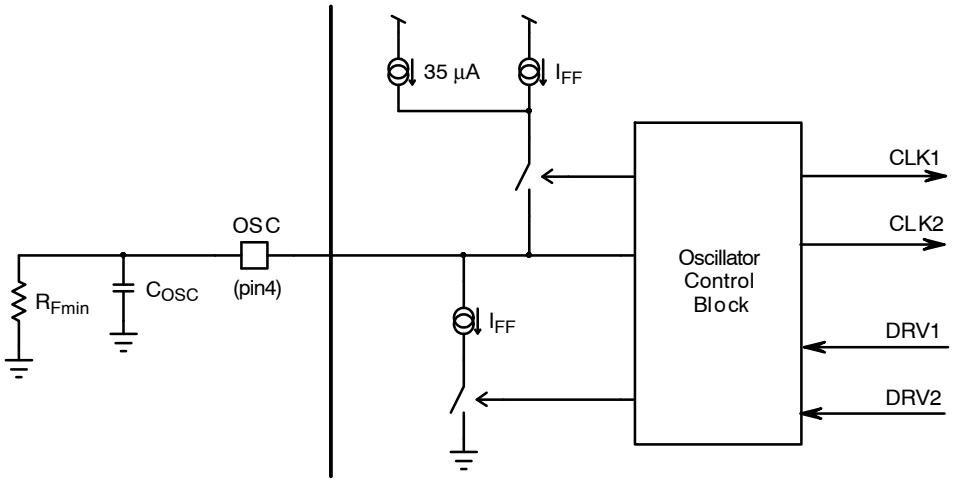


Figure 5. Adjustment of the Minimum Frequency

Assuming that the internal I_{FF} current is zero, the oscillator period can be computed considering the 35−μA charge current, the permanent leakage current generated by R_{Fmin} and the 1 V swing across C_{OSC} (swing when the oscillator is clamping the switching frequency).

Doing this calculation, we can deduce the minimum clamp frequency (for each branch) forced by R_{Fmin}:

$$\left(f_{sw(max)}\right)_{min} = \frac{f_{OSC(min)}}{2} = \frac{1}{2 \cdot R_{Fmin} \cdot C_{OSC} \cdot \left(0.22 + \ln\left(\frac{R_{Fmin} - 114000}{R_{Fmin} - 143000}\right)\right)} \quad \text{(eq. 16)}$$

In our application, (R_{Fmin} = 270 kΩ) forces a minimum frequency of about 20 kHz.

Remark: Ground pin6 to inhibit the frequency foldback. If pin6 is grounded (accidently or not), the circuit operates with the nominal clamp frequency over the whole load range.

Brown−out Circuitry

The brown−out terminal (pin7) typically receives a portion of the PFC input voltage (V_{IN}). As during the PFC operation, V_{IN} is a rectified sinusoid, a capacitor must integrate the ac line ripple so that a portion of the (V_{IN}) average value is applied to the brown−out pin.

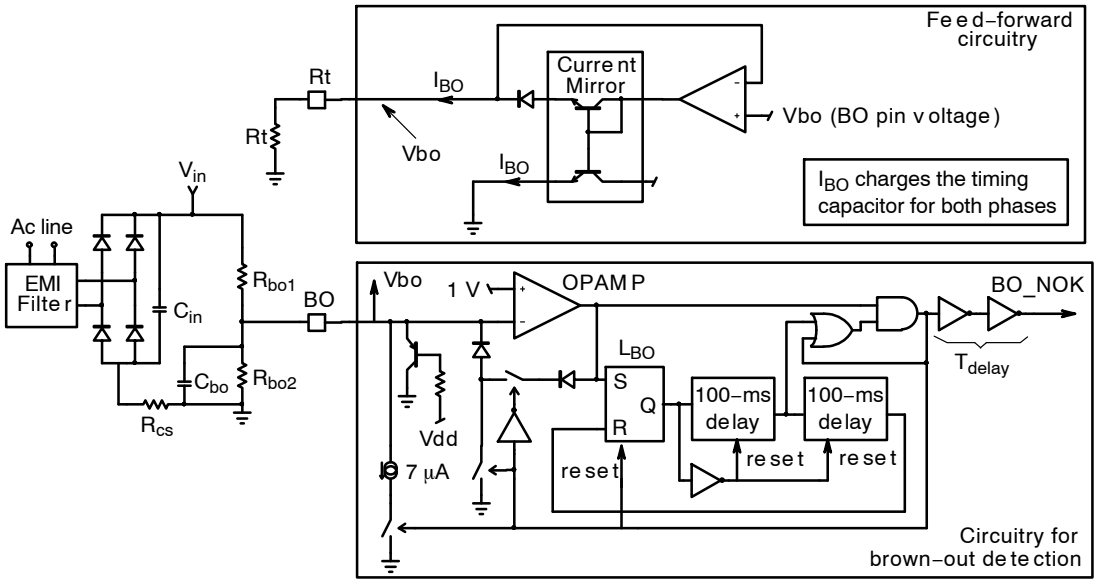


Figure 6. Brown−out Block

As sketched by Figure 6, the brown−out block has two functions:

1. Feed−forward: The brown−out pin voltage is buffered to generate an internal current I_{BO} proportional to the input voltage average value in conjunction with the pin3 resistor (R_t). This current is squared to form the current that charges the internal timing capacitors that control the on−time in the two branches. As a matter of fact, the on−time is inversely proportional to the square of the line magnitude. This feed−forward feature makes the transfer function and the power delivery independent of the ac line level.
2. Detection of the line magnitude being too low. A 7−μA current source lowers the BO pin voltage when a brown−out condition is detected, for hysteresis purpose as required by this function. In traditional applications, the sensed voltage dramatically varies depending on the PFC stage state:
   - Before operation, the PFC stage is off and the input bridge acts as a peak detector (refer to Figure 7). As a consequence, the input voltage is approximately flat and nearly equates the ac line amplitude:

$$V_{IN} = \sqrt{2} \cdot V_{in,rms}$$

   where $V_{in,rms}$ is the rms voltage of the line. Hence, the voltage applied to pin7 is:

$$V_{pin7} = \sqrt{2} \cdot V_{in,rms} \cdot \frac{R_{bo2}}{R_{bo1} + R_{bo2}}$$

   - After the PFC stage has started operation, the input voltage becomes a rectified sinusoid and the voltage applied to pin7 is:

$$V_{pin7} = \frac{2 \cdot \sqrt{2} \cdot V_{in,rms}}{\pi} \frac{R_{bo2}}{R_{bo1} + R_{bo2}}$$

   i.e., about 64% of the previous value.

Therefore, in traditional applications, the same line magnitude leads to a BO pin voltage that is 36% lower when the PFC is working. That is why a large hysteresis is required.

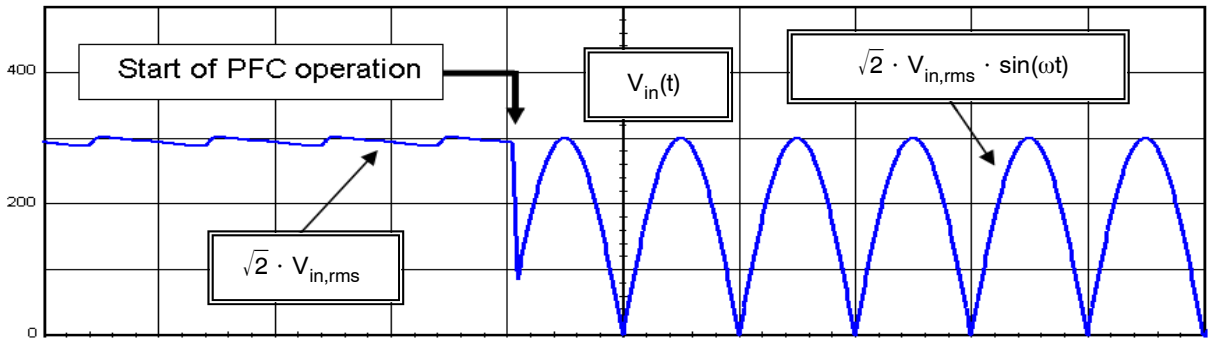


Figure 7. Typical Input Voltage of a PFC Stage

Computing C_{bo}, R_{bo1} and R_{bo2} of Figure 6:

1. Define the line levels at which the circuit should detect a brown−out and recover operation:

Our application being specified to operate from 90 V_{rms}, it can make sense to select the following thresholds:

- The system starts operating when the line voltage is above $(V_{in,rms})_{boH}$ = 81 V (90% of 90 V)
- The system detects a fault when the line voltage goes below $(V_{in,rms})_{boL}$ = 72 V (80% of 90 V)

1. Define the average input voltage when V_{pin7} (BO pin voltage) crosses the BO thresholds (V_{pin7} rising and falling):

When the line voltage is below the BO threshold, the internal current source (I_{HYST} = 7 μA, typically) is activated to offer some hysteresis and the circuit recovers operation when:

$$\frac{R_{bo2}}{R_{bo1} + R_{bo2}} \cdot \left(V_{in,avg}\right)_{boH} - \left(\frac{R_{bo1} \cdot R_{bo2}}{R_{bo1} + R_{bo2}} \cdot I_{HYST}\right) = V_{bo(th)} \quad \text{(eq. 17)}$$

Where $(V_{in,avg})_{boH}$ is the average input voltage above which the circuit turns on and $V_{bo(th)}$ is the BO internal threshold (1 V typically).

Hence:

$$\left(V_{in,avg}\right)_{boH} = \left(\frac{R_{bo1} + R_{bo2}}{R_{bo2}} \cdot V_{bo(th)}\right) + \left(R_{bo1} \cdot I_{HYST}\right) \quad \text{(eq. 18)}$$

As long as the line is above the BO threshold, the internal current source (I_{HYST} = 7 μA typically) is off and the BO pin voltage is:

$$V_{pin7} = k_{BO} \cdot V_{in,avg} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right) \quad \text{(eq. 19)}$$

Where:

- ($V_{in,avg}$) is the average input voltage
- f_{line} is the line frequency
- f_{BO} is the sensing network pole frequency

$$\left(f_{BO} = \frac{R_{bo1} + R_{bo2}}{2\pi \cdot R_{bo1} \cdot R_{bo2} \cdot C_{bo}}\right)$$

- k_{BO} is scale down factor of the BO sensing network

$$\left(k_{BO} = \frac{R_{bo2}}{R_{bo1} + R_{bo2}}\right)$$

The term

$$\left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)$$

of Equation 19 enables to take into account the BO pin voltage ripple (first harmonic approximation).

A brown−out fault is detected when the BO pin voltage goes below $V_{bo(th)}$ (BO internal threshold that is 1 V typically). Hence, the BO protection triggers when the average voltage goes below the $(V_{in,avg})_{boL}$ level expressed by the following equation:

$$\left(V_{in,avg}\right)_{boL} = \frac{V_{BO(th)}}{k_{BO} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)} \quad \text{(eq. 20)}$$

Where $(V_{in,avg})_{boL}$ is the average input voltage below which the circuit turns off, f_{BO} is the sensing network pole frequency

$$\left(f_{BO} = \frac{R_{bo1} + R_{bo2}}{2\pi \cdot R_{bo1} \cdot R_{bo2} \cdot C_{bo}}\right)$$

and f_{line} is the line frequency.

2. Calculation

From Equation 20, we can deduce the following expression of the brown−out scale down factor:

$$K_{BO} = \frac{R_{bo2}}{R_{bo1} + R_{bo2}} = \frac{V_{BO(th)}}{(V_{in,avg})_{boL} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)} \quad \text{(eq. 21)}$$

Substitution of Equation 21 into Equation 18 leads to:

$$(V_{in,avg})_{boH} = \left((V_{in,avg})_{boL} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)\right) + (R_{bo1} \cdot I_{HYST}) \quad \text{(eq. 22)}$$

We can then deduce the following expression of R_{bo1}:

$$R_{bo1} = \frac{(V_{in,avg})_{boH} - \left((V_{in,avg})_{boL} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)\right)}{I_{HYST}} \quad \text{(eq. 23)}$$

Re−using the above R_{bo1} expression, one can deduce R_{bo2} from Equation 21:

$$R_{bo2} = \frac{R_{bo1}}{\left(\frac{(V_{in,avg})_{boL}}{V_{BO(th)}} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)\right) - 1} \quad \text{(eq. 24)}$$

If as a rule of the thumb, we will assume that

$$\left(f_{BO} = \frac{f_{line}}{10}\right)$$

that is 6 Hz in the case of a 60−Hz line, we obtain:

$$R_{bo1} = \frac{(V_{in,avg})_{boH} - \left[(V_{in,avg})_{boL} \cdot \left|1 - \frac{\frac{f_{line}}{10}}{3 \cdot f_{line}}\right|\right]}{I_{HYST}} \cong \frac{(V_{in,avg})_{boH} - \left(0.967 \cdot (V_{in,avg})_{boL}\right)}{I_{HYST}} \quad \text{(eq. 25)}$$

$$R_{bo2} = \frac{R_{bo1}}{\left(\frac{(V_{in,avg})_{boL}}{V_{BO(th)}} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)\right) - 1} \cong \frac{R_{bo1}}{\left(0.967 \cdot \frac{(V_{in,avg})_{boL}}{V_{BO(th)}}\right) - 1} \quad \text{(eq. 26)}$$

As an example, we will consider the traditional PFC stage where the average value of the input voltage is 36% lower when the circuit operates (as illustrated by Figure 7).

So if we select:

- The system starts operating when the line voltage is above

$$(V_{in,rms})_{boH} = 81\ V$$

- The system detects a fault when the line voltage goes below

$$(V_{in,rms})_{boL} = 72\ V$$

The corresponding average input voltage thresholds are:

$$(V_{in,avg})_{boH} = \sqrt{2} \cdot (V_{in,rms})_{boH} = \sqrt{2} \cdot 81 \quad \text{(eq. 27)}$$

And:

$$(V_{in,avg})_{boL} = \frac{2\sqrt{2}}{\pi} \cdot (V_{in,rms})_{boL} = \frac{2\sqrt{2}}{\pi} \cdot 72 \quad \text{(eq. 28)}$$

We have then to solve:

$$R_{bo1} \cong \frac{\left(\sqrt{2} \cdot 81\right) - \left(0.967 \cdot \frac{2\sqrt{2}}{\pi} \cdot 72\right)}{7 \cdot 10^{-6}} \cong 7410\ k\Omega \quad \text{(eq. 29)}$$

$$R_{bo2} \cong \frac{7410 \cdot 10^3}{\left(\frac{0.967 \cdot \frac{2\sqrt{2}}{\pi} \cdot 72}{1}\right) - 1} \cong 120\ k\Omega \quad \text{(eq. 30)}$$

$$C_{bo} = \frac{R_{bo1} + R_{bo2}}{2\pi \cdot R_{bo1} \cdot R_{bo2} \cdot \frac{f_{line}}{10}} \cong \frac{7410\ k + 120\ k}{2\pi \cdot 7410\ k \cdot 120\ k \cdot \frac{60}{10}} \cong 225\ nF \quad \text{(eq. 31)}$$

In practice, four 1.8−MΩ resistors are placed in series for $\boldsymbol{R_{bo1}}$ (for a global 7.2−MΩ resistor) and we use a 120−kΩ resistor for $\boldsymbol{R_{bo2}}$ and 220−nF capacitor for $\boldsymbol{C_{bo}}$.

One should note that the NCP1631 brown−out circuitry incorporates a 50−ms blanking delay to help meet hold−up times requirement (see data sheet).

Maximum Power Adjustment

The instantaneous line current is the averaged value (over the switching frequency) of the total current absorbed by the two branches of the PFC stage. It is given by the following formula:

$$I_{in}(t) = \frac{V_{in}(t)}{L} \cdot \frac{(R_t)^2 \cdot V_{REGUL}}{26.9 \cdot 10^{12} \cdot {k_{BO}}^2 \cdot {V_{in,rms}}^2} \quad \text{(eq. 32)}$$

Where:

$$\left(\frac{(R_t)^2 \cdot V_{REGUL}}{26.9 \cdot 10^{12} \cdot k_{BO}{}^2 \cdot V_{in,rms}{}^2}\right)$$

is the expression of the on−time in each branch

- (V_{REGUL}) is an internal signal linearly dependent of the output of the regulation block ($V_{CONTROL}$). (V_{REGUL}) varies between 0 and 1.66 V.
- $I_{in}(t)$ and $V_{in}(t)$ are the instantaneous line current and voltage respectively.
- $V_{in,rms}$ is the line rms voltage
- L is the coil inductance
- k_{BO} is scale down factor of the BO sensing network

$$\left(k_{BO} = \frac{R_{bo2}}{R_{bo1} + R_{bo2}}\right)$$

Multiplying I_{in} by V_{in}, one can deduce the instantaneous power:

$$P_{in}(t) = \frac{(R_t)^2 \cdot V_{REGUL} \cdot V_{in}{}^2(t)}{26.9 \cdot 10^{12} \cdot L \cdot k_{BO}{}^2 \cdot V_{in,rms}{}^2} \qquad \text{(eq. 33)}$$

And averaging the instantaneous power over the line period gives the following expression of the mean input power:

$$P_{in,avg} = \frac{(R_t)^2 \cdot V_{REGUL}}{26.9 \cdot 10^{12} \cdot L \cdot k_{BO}{}^2} \qquad \text{(eq. 34)}$$

As a result of the feed−forward, the delivered power does not depend on the line magnitude but is the only function of the coil inductance, of the input voltage sensing network (used and dimensioned for the brown−out detection) and of R_t capacitor, that is, the timing resistor that is applied to pin3.

Since V_{REGUL} is clamped to 1.66 V, the maximum power ($(P_{in})_{HL}$) that can be virtually delivered by the PFC stage is:

$$(P_{in})_{HL} = \frac{(R_t)^2 \cdot 1.66}{26.9 \cdot 10^{12} \cdot L \cdot k_{BO}{}^2} \cong \frac{(R_t)^2}{16.2 \cdot 10^{12} \cdot L \cdot k_{BO}{}^2} \qquad \text{(eq. 35)}$$

Hence:

$$R_t \cong 4025 \cdot 10^3 \cdot k_{BO} \cdot \sqrt{L \cdot (P_{in})_{HL}} \qquad \text{(eq. 36)}$$

For the sake of a welcome margin, ($(P_{in})_{HL}$) should be selected about 25% higher than the expected maximal input power that is: (125% x 325 W ≅ 400 W) in the application of interest.

In our case,

- L = 150 μH
- Since R_{bo1} = 7200 kΩ and R_{bo2} = 120 kΩ,

$$\left(k_{BO} = \frac{R_{bo2}}{R_{bo1} + R_{bo2}} = \frac{1}{61}\right)$$

Hence:

$$R_t \cong 4025 \cdot 10^3 \cdot \frac{1}{61} \cdot \sqrt{150 \cdot 10^{-6} \cdot 400} \cong 16 \cdot 2\ k\Omega \qquad \text{(eq. 37)}$$

A 18−kΩ resistor is selected that leads to

$$(P_{in})_{HL} = \frac{(18 \cdot 10^3)^2 \cdot 61^2}{16.2 \cdot 10^{12} \cdot 150 \cdot 10^{-6}} \cong 496\ W$$

Feed−back Network

The NCP1631 embeds a trans−conductance error amplifier that typically features a 200−μS trans−conductance gain and a ±20−μA maximum capability (see Figure 8). The output voltage of the PFC stage is externally scaled down by a resistors divider and monitored by the feed−back input (pin2). The bias current is minimized (less than 500 nA) to allow the use of a high impedance feed−back network. The output of the error amplifier is pinned out for external loop compensation (pin5).

Computation of the Feed−back / Regulation External Components

A resistor divider consisting of R_{fb1} and R_{fb2} of Figure 8 must provide pin2 with a voltage proportional to the PFC output voltage so that V_{pin2} equates the internal reference voltage (V_{REF} = 2.5 V) when the PFC output voltage is nominal. In other words:

$$\frac{R_{fb2}}{R_{fb1} + R_{fb2}} \cdot V_{out,nom} = V_{REF} \qquad \text{(eq. 38)}$$

Or:

$$\frac{R_{fb1}}{R_{fb2}} = \frac{V_{out,nom}}{V_{REF}} - 1 \qquad \text{(eq. 39)}$$

Another constraint on the feed−back resistors is the power it dissipates. R_{fb1} and R_{fb2} being biased by the PFC output high voltage (in the range of 390 V typically), they can easily consume several hundreds of mW if their resistance is low. Targeting a bias current in the range of 100 μA generally gives a good trade−off between losses and noise immunity.

This criterion leads to:

$$R_{fb2} = \frac{V_{REF}}{100\ \mu A} = 25\ k\Omega \qquad \text{(eq. 40)}$$

In practice, (R_{fb2} = 27 kΩ) was selected for our application.

Following Equation 39, R_{fb1} is given by:

$$R_{fb1} = R_{fb2} \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1\right) \qquad \text{(eq. 41)}$$

We target a 390−V regulation level, hence:

$$R_{fb1} = 27\ k\Omega \cdot \left(\frac{390}{2.5} - 1\right) = 4185\ k\Omega \qquad \text{(eq. 42)}$$

Like for the input voltage sensing network, several resistors should be placed in series instead of a single R_{fb1} resistor. In our application, we choose a (1800 kΩ + 1800 kΩ + 560 kΩ) network. This selection together with (R_{fb2} = 27 kΩ) leads to:

$$V_{out,nom} = \frac{R_{fb1} + R_{fb2}}{R_{fb2}} \cdot V_{REF} = \frac{1800\ k + 1800\ k + 560\ k + 27\ k}{27\ k} \cdot 2.5\ V \cong 388\ V \qquad \text{(eq. 43)}$$

Compensation:

The NCP1631 uses the brown−out input voltage to provide some feed−forward. This allows the small−signal transfer function of PFC stage to be independent of the ac line amplitude. More specifically, the bulk capacitor ESR being neglected:

$$\frac{\hat{V}_{out}}{\hat{V}_{REGUL}} = \frac{(R_t)^2 \cdot R_{out}}{53.8 \cdot 10^{12} \cdot L \cdot k_{BO}{}^2 \cdot V_{out,nom}} \cdot \frac{1}{1 + \left(s \cdot \frac{R_{out} \cdot C_{bulk}}{2}\right)} \qquad \text{(eq. 44)}$$

Where:

- C_{bulk} is the bulk capacitor.
- R_{out} is the load equivalent resistance.
- R_t is the pin3 external capacitor.
- L is the PFC coil inductance.
- K_{BO} is the brown−out scale−down factor.
- $V_{out,nom}$ is the regulation level of the PFC output.

However, PFC stages must exhibit a very low regulation bandwidth, in the range of or lower than 20 Hz to yield high power factor ratios. Hence, sharp variations of the load generally result in excessive over and under−shoots. The NCP1631 limits over−shoots by the Over−Voltage Protection (see OVP section). To contain under−shoots, an internal comparator monitors the feed−back (V_{pin2}) and when V_{pin2} is lower than 95.5% of its nominal value, it connects a 220−μA current source to speed−up the charge of the compensation capacitors. Finally, it is like if the comparator multiplied the error amplifier gain by about 10 (Note 1).

The implementation of this ***dynamic response enhancer*** together with the accurate and programmable over−voltage protection, guarantees a reduced spread of the output voltage in all conditions included sharp line / load transients.

Hence, in most applications, it can be sufficient to place a low frequency pole that drastically limits the bandwidth. However, it is recommended to implement a type2 compensation as represented by the following figure:

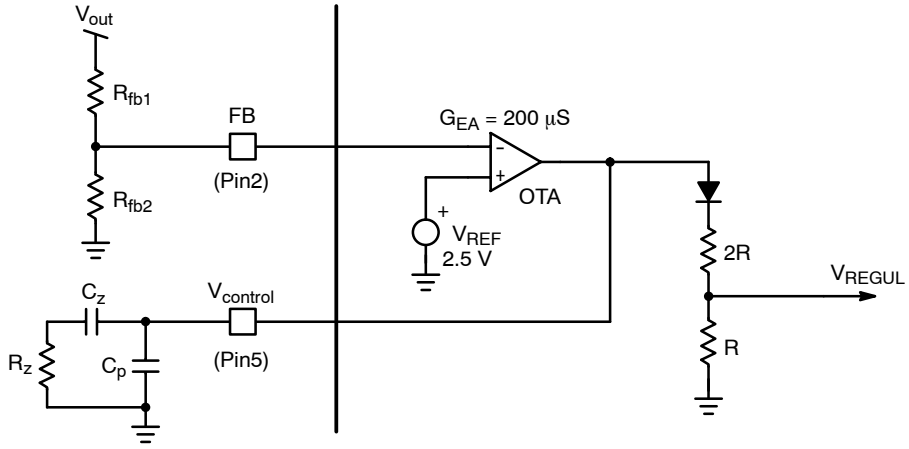


Figure 8. Regulation Trans−conductance Error Amplifier, Feed−back and Compensation Network

1. The circuit disables this capability (dynamic response enhancer) until the PFC stage output voltage has reached its target level (that is when the “pfcOK” signal of the block diagram, is high). This is because, at the beginning of operation, the pin5 compensation network must charge slowly and gradually for a soft start−up.

The output to control transfer function brought by the type−2 compensator is:

$$\frac{\hat{V}_{control}}{\hat{V}_{out}} = \frac{1 + sR_zC_z}{sR_o(C_z + C_p)\left(1 + sR_z\frac{C_z \cdot C_p}{C_z + C_p}\right)} \quad \text{(eq. 45)}$$

$$\text{Where} \quad R_0 = \frac{V_{out,nom}}{V_{ref} \cdot G_{EA}} \ ,$$

G_{EA} being the gain of the trans−conductance error amplifier (OTA), $V_{out,nom}$, the output nominal voltage (V_{out} regulation level) and V_{REF}, the OTA 2.5−V voltage reference.

Actually, The NCP1631 PWM section does not directly use $V_{control}$ but V_{REGUL}. Taking into the (5/9) resistors divider that links $V_{control}$ and V_{REGUL}, it comes:

$$\frac{\hat{V}_{REGUL}}{\hat{V}_{out}} = \frac{1 + sR_zC_z}{s\frac{9 \cdot R_o}{5} \cdot (C_z + C_p)\left(1 + sR_z\frac{C_z \cdot C_p}{C_z + C_p}\right)} \quad \text{(eq. 46)}$$

Hence, we have:

$$\frac{\hat{V}_{REGUL}}{\hat{V}_{out}} = \frac{1 + \frac{s}{2\pi \cdot f_z}}{\frac{s}{2\pi \cdot f_{p0}}\left(1 + \frac{s}{2\pi \cdot f_{p1}}\right)} \quad \text{(eq. 47)}$$

Where:

- f_z is the frequency of the compensator zero:

$$f_z = \frac{1}{2\pi \cdot R_z \cdot C_z}$$

- f_{p1} is the frequency of the compensator high frequency pole:

$$f_{p1} = \frac{1}{2\pi \cdot R_z \cdot \left(\frac{C_p \cdot C_z}{C_p + C_z}\right)}$$

- f_{p0} is the frequency of the origin pole:

$$f_{p0} = \frac{5}{18\pi \cdot R_0 \cdot (C_p + C_z)}$$

- $R_0 = \frac{V_{out,nom}}{V_{ref} \cdot G_{EA}}$

Place the zero and the high frequency pole

We can obtain a 60° phase boost and hence, a 60° phase margin by placing the compensation zero at (f_c/4) and the high frequency pole at (4 x f_c), where f_c is the selected crossover frequency.

From this, it comes that:

$$f_{p1} = 4^2 \cdot f_z \quad \text{(eq. 48)}$$

Substitution of the f_{p1} and f_z expressions into Equation 48 leads to:

$$\frac{C_p \cdot C_z}{C_p + C_z} = \frac{C_z}{16} \quad \text{(eq. 49)}$$

Hence:

$$C_z = 15 \cdot C_p \quad \text{(eq. 50)}$$

Place the pole at the origin to have the proper bandwidth:

Equation 44 instructs that the static gain of the PFC boost is:

$$G_o = \frac{(R_t)^2 \cdot R_{out}}{53.8 \cdot 10^{12} \cdot L \cdot k_{BO}{}^2 \cdot V_{out,nom}} \quad \text{(eq. 51)}$$

If f_c is the desired crossover frequency, the pole at the origin must be placed at the load that would set the boost converter pole at the selected compensation zero. Hence:

$$-20 \cdot \log\left(\frac{f_c}{f_{p0}}\right) = -20 \cdot \log\left(G \,\middle|\, \left(R_{out} = \frac{4}{\pi \cdot C_{bulk} \cdot f_c}\right)\right) \quad \text{(eq. 52)}$$

Or:

$$f_{p0} = \frac{f_c}{G_0 \,\middle|\, R_{out} = \frac{4}{\pi \cdot C_{bulk} \cdot f_c}} \quad \text{(eq. 53)}$$

This leads to:

$$f_{p0} = \frac{\frac{f_c}{4 \cdot R_t{}^2}}{\pi \cdot 53.8 \cdot 10^{12} \cdot L \cdot C_{bulk} \cdot k_{BO}{}^2 \cdot f_c \cdot V_{out,nom}} \quad \text{(eq. 54)}$$

This expression simplifies as follows:

$$f_{p0} = \frac{\pi \cdot 53.8 \cdot 10^{12} \cdot L \cdot C_{bulk} \cdot k_{BO}{}^2 \cdot f_c{}^2 \cdot V_{out,nom}}{4 \cdot R_t{}^2} \quad \text{(eq. 55)}$$

Where:

k_{BO} is scale down factor of the BO sensing network

$$\left(k_{BO} = \frac{R_{bo2}}{R_{bo1} + R_{bo2}}\right)$$

Replacing f_{p0} by its expression of Equation 55, it comes:

$$\frac{5}{18\pi \cdot R_0 \cdot (C_p + C_z)} = \frac{5}{18\pi \cdot \left(\frac{V_{out,nom}}{V_{ref} \cdot G_{EA}}\right) \cdot (16 \cdot C_p)} = \frac{\pi \cdot 53.8 \cdot 10^{12} \cdot L \cdot C_{bulk} \cdot k_{BO}{}^2 \cdot f_c{}^2 \cdot V_{out,nom}}{4 \cdot R_t{}^2} \quad \text{(eq. 56)}$$

Replacing G_{EA} and V_{ref} by their typical value (200 μS and 2.5 V, respectively, we can write the following equation that gives C_p:

$$C_p \cong \frac{V_{ref} \cdot G_{EA} \cdot R_t{}^2}{7646.2 \cdot 10^{12} \cdot L \cdot C_{bulk} \cdot k_{BO}{}^2 \cdot f_c{}^2 \cdot (V_{out,nom})^2} \quad \text{(eq. 57)}$$

Replacing R_t by this expression of Equation 36, the precedent equation simplifies:

$$C_p \cong \frac{1.06 \cdot 10^{-6} \cdot (P_{in})_{HL}}{C_{bulk} \cdot f_c{}^2 \cdot (V_{out,nom})^2} \quad \text{(eq. 58)}$$

Computing R_z:

The compensation zero being placed at (f_c/4), it comes:

$$f_z = \frac{1}{2\pi \cdot R_z \cdot C_z} = \frac{f_c}{4} \quad \text{(eq. 59)}$$

Finally, from the above computations, we can deduce the following equations to design the compensation network.

$$C_p \cong \frac{1.06 \cdot 10^{-6} \cdot (P_{in})_{HL}}{C_{bulk} \cdot f_c{}^2 \cdot (V_{out,nom})^2} \quad \text{(eq. 60)}$$

$$C_z = 15 \cdot C_p \quad \text{(eq. 61)}$$

$$R_z = \frac{2}{\pi \cdot C_z \cdot f_c} \quad \text{(eq. 62)}$$

In our application,

$$C_p = \frac{1.06 \cdot 10^{-6} \cdot 497}{100 \cdot 10^{-6} \cdot 20^2 \cdot 390^2} \cong 86 \text{ nF} \quad \text{(eq. 63)}$$

Practically, we will use 68−nF capacitor that is a close standard value.

$$C_z = 15 \cdot C_p = 1020 \text{ nF} \quad \text{(eq. 64)}$$

In practice, a 1−μF standard capacitor is selected.
Finally,

$$R_z = \frac{2}{\pi \cdot 1 \cdot 10^{-6} \cdot 20} \cong 31.8 \text{ k}\Omega \quad \text{(eq. 65)}$$

A 33−kΩ resistor is implemented.

The compensation is computed to have a phase margin in the range of 60°. The high frequency pole can be set at a lower frequency. Practically, C_p can be increased up to 4 times the proposed value (without changing $\boldsymbol{R_z}$ and $\boldsymbol{C_z}$) to reduce the ripple on the $\boldsymbol{V_{control}}$ pin and further improve the THD. The crossover frequency is unchanged. This is just at the cost of a diminution of the phase margin that can drop as low as 30°. More specifically:

$$\Phi_m = \arctan\left(\frac{f_c}{f_z}\right) - \arctan\left(\frac{f_c}{f_{p1}}\right) \quad \text{(eq. 66)}$$

Where:

- f_z is the frequency of the compensator zero:

$$f_z = \frac{1}{2\pi \cdot R_z \cdot C_z}$$

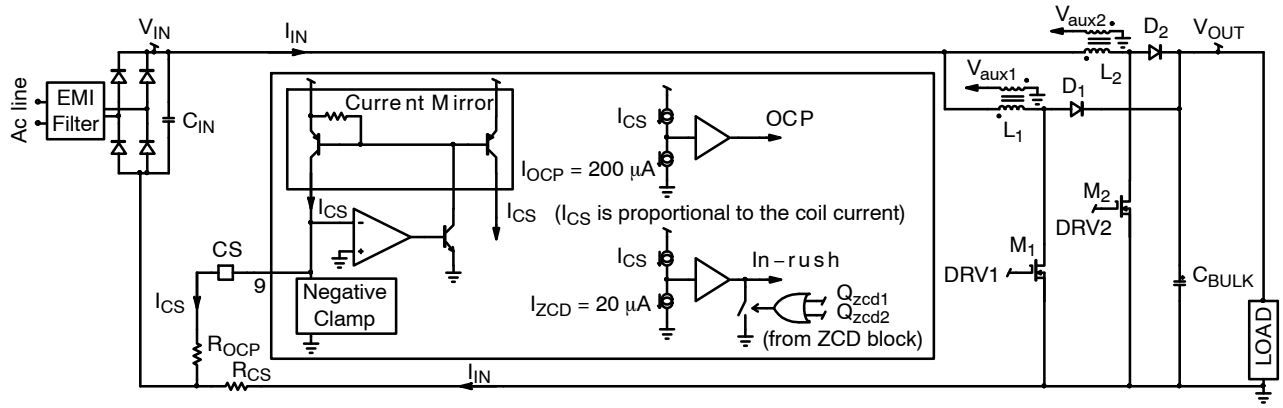
- f_{p1} is the frequency of the compensator high frequency pole:

$$f_{p1} = \frac{1}{2\pi \cdot R_z \cdot \left(\frac{C_p \cdot C_z}{C_p + C_z}\right)}$$

Finally, a 150−nF capacitor is selected for $\boldsymbol{C_p}$, leading to:

$$(f_z \cong 5 \text{ Hz}),\ (f_{p1} \cong 37 \text{ Hz}),\ (\Phi_m \cong 76° - 28° = 48°)$$

Current Sense Network



The CS block performs the over−current protection and detects the in−rush currents

Figure 9. Current Sense Block

The NCP1631 is designed to monitor a negative voltage proportional to the coil current. Practically, a current sense resistor (***R_CS*** of Figure 9) is inserted in the return path to generate a negative voltage proportional to the total current absorbed by the two branches. The circuit incorporates an operational amplifier that sources the current necessary to maintain the CS pin voltage null (refer to Figure 9). By inserting a resistor ***R_OCP*** between the CS pin and ***R_CS***, we adjust the pin9 current as follows:

$$-(R_{CS} \cdot I_{in}) + (R_{OCP} \cdot I_{pin9}) = V_{pin9} \cong 0 \qquad \text{(eq. 67)}$$

Which leads to:

$$I_{CS} = I_{pin9} = \frac{R_{CS}}{R_{OCP}} I_{in} \qquad \text{(eq. 68)}$$

Where ***I_in*** is the total current drawn by the two phases of the interleaved PFC stage.

The circuit compares ***I_CS*** to an internal 210−μA current reference for a cycle by cycle current limitation. Hence, the maximum coil current is:

$$I_{in,max} = \frac{R_{OCP}}{R_{CS}} \cdot 210\ \mu A \qquad \text{(eq. 69)}$$

Finally, the ratio (***R_OCP*** / ***R_CS***) sets the over−current limit in accordance with the following equation:

$$\frac{R_{OCP}}{R_{CS}} = \frac{I_{in,max}}{210\ \mu A} \qquad \text{(eq. 70)}$$

As we have two external components to set the current limit (***R_OCP*** and ***R_CS***), the current sense resistor can be optimized to have the ***best trade−off between losses and noise immunity***.

- Maximum current drawn by the two branches:

As shown in [1], the following equations give the total current that is absorbed by the interleaved PFC.

$$I_{in,max} = 2\sqrt{2} \cdot \frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}} \cdot \left[1 - \frac{V_{out,nom}}{4 \cdot \left(V_{out,nom} - \left(\sqrt{2} \cdot (V_{in,rms})_{LL}\right)\right)}\right] \text{ if } (V_{in,rms})_{LL} \le \frac{V_{out,nom}}{2\sqrt{2}} \qquad \text{(eq. 71)}$$

$$I_{in,max} = 2\sqrt{2} \cdot \frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}} \cdot \left(1 - \frac{V_{out,nom}}{4 \cdot \sqrt{2} \cdot (V_{in,rms})_{LL}}\right) \text{ if } (V_{in,rms})_{LL} \ge \frac{V_{out,nom}}{2\sqrt{2}} \qquad \text{(eq. 72)}$$

Where:

- ***(V_in,rms)_LL*** is the lowest level of the line rms voltage.
- ***(P_in,avg)_max*** is the maximum level of the input power.
- ***V_out,nom*** is the nominal level of the output voltage (or the output regulation voltage)

In our case,

$$\left((V_{in,rms})_{LL} = 90 \le \frac{V_{out,nom}}{2\sqrt{2}} = \frac{390}{2\sqrt{2}} \cong 138\right)$$

Hence:

$$I_{in,max} = 2\sqrt{2} \cdot \frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}} \cdot \left[1 - \frac{V_{out,nom}}{4 \cdot \left(V_{out,nom} - \left(\sqrt{2} \cdot (V_{in,rms})_{LL}\right)\right)}\right] \quad \text{(eq. 73)}$$

$$I_{in,max} = 2\sqrt{2} \cdot \frac{325}{90} \cdot \left[1 - \frac{390}{4 \cdot \left(390 - \left(\sqrt{2} \cdot 90\right)\right)}\right] \cong 6.4\ A \quad \text{(eq. 74)}$$

- Selecting $\boldsymbol{R_{OCP}}$ and $\boldsymbol{R_{CS}}$:

If we neglect the input current ripple, the $\boldsymbol{R_{CS}}$ losses are given by the following simplified equation:

$$P_{Rcs} = R_{CS} \cdot \left(\frac{P_{in,avg}}{V_{in,rms}}\right)^2 \quad \text{(eq. 75)}$$

One can choose $\boldsymbol{R_{CS}}$ as a function of its relative impact on the PFC stage efficiency at low line and full power. If α is the relative percentage of the power that can be consumed by $\boldsymbol{R_{CS}}$, this criterion leads to:

$$\propto \cdot (P_{in,avg})_{max} = R_{CS} \cdot \left(\frac{(P_{in,avg})_{max}}{(V_{in,rms})_{min}}\right)^2 \quad \text{(eq. 76)}$$

Finally:

$$R_{CS} = \propto \cdot \frac{(V_{in,rms})_{min}{}^2}{(P_{in,avg})_{max}} \quad \text{(eq. 77)}$$

And:

$$R_{OCP} = R_{CS} \cdot \frac{I_{in,max}}{210\ \mu A} \quad \text{(eq. 78)}$$

Generally (α = 0.2%) gives a good trade−off between losses and noise immunity (0.2% of the power is lost in the $\boldsymbol{R_{CS}}$ at low line).

This criterion leads to the following $\boldsymbol{R_{CS}}$ value:

$$R_{cs} = 0.2\% \cdot \frac{90^2}{325} \cong 50\ m\Omega \quad \text{(eq. 79)}$$

This selection results in the following $\boldsymbol{R_{OCP}}$ resistor:

$$R_{OCP} = 50\ m \cdot \frac{6.4\ A}{210\ \mu A} \cong 1.5\ k\Omega \quad \text{(eq. 80)}$$

Zero Current Detection (ZCD)

For each phase, a winding taken off of the boost inductor gives the zero current detection (ZCD) information. When the switch is on, the ZCD pin voltage is equal to:

$$V_{zcd} = -\frac{V_{in}}{N} \quad \text{(eq. 81)}$$

Where $\boldsymbol{V_{in}}$ is the instantaneous ac line voltage and $\boldsymbol{N}$, the turns ratio (ratio number of turns of the primary winding over the number of turns of the ZCD auxiliary winding)

When the switch is off, the ZCD pin voltage is equal to:

$$V_{zcd} = \frac{V_{out} - V_{in}}{N} \quad \text{(eq. 82)}$$

The NCP1631 incorporates two ZCD comparators:

1. A first one senses pin1 that is to receive the ZCD voltage from branch 2
2. A second one monitors pin16 that receives the ZCD signal for branch1.

The ZCD comparators have a 0.5−V threshold (rising, with a 250−mV hysteresis). Therefore, $\boldsymbol{N}$ must be sized such that at least 0.5 V is obtained on the ZCD pin during the demagnetization in all operating conditions. The voltage obtained on the ZCD pin is minimal in high line and at the top of the sinusoid, leading to:

$$N \leq \frac{V_{out} - \left(\sqrt{2} \cdot (V_{in,rms})_{HL}\right)}{0.5}$$

With ($(V_{in,rms})_{HL}$ = 265 V) and (V_{out} = 390 V), ***N*** must be lower than 30. A turns ratio of 10 was selected for this design.

A resistor, $\boldsymbol{R_{ZCD}}_1$ is to be added between the phase 1 ZCD winding and pin 16 for branch 1 and another one $\boldsymbol{R_{ZCD}}_2$ between the phase 2 ZCD winding and pin1 for branch 2. $\boldsymbol{R_{ZCD}}_1$ and $\boldsymbol{R_{ZCD}}_2$ limit the current into or out of pins 1 and 16. This current is preferably set in the range of 2 mA (sink and source). In general, the pins are the most stressed by the sink current obtained at high line. Hence, $\boldsymbol{R_{ZCD}}_1$ and $\boldsymbol{R_{ZCD}}_2$ must be selected high enough so that:

$$R_{ZCD1} = R_{ZCD2} \geq \frac{\sqrt{2} \cdot (V_{in,rms})_{HL}}{I_{ZCD} \cdot N} = \frac{\sqrt{2} \cdot 265}{2\ m \cdot 10} \cong 19\ k\Omega \quad \text{(eq. 83)}$$

A 22−kΩ was selected.

However, the value of this resistor and the small parasitic capacitance of the ZCD pin also determine when the ZCD winding information is detected and the next drive pulse begins. Ideally, the ZCD resistor will restart the drive at its valley. This will minimize switching losses by turning the MOSFET back on when its drain voltage is at a minimum. The value of $\boldsymbol{R_{ZCD}}_1$ and $\boldsymbol{R_{ZCD}}_2$ to accomplish this is best found experimentally. Too high of a value could create a significant delay in detecting the ZCD event. In this case, the controller would operate in discontinuous conduction mode (DCM) and the power factor would suffer. Conversely, if the ZCD resistor is too low, then the next driver pulse would start when the voltage is still high and switching efficiency would suffer.

Over−Voltage Protection

The NCP1631 dedicates one specific pin for the under−voltage and over−voltage protections. The NCP1631 configuration allows the implementation of two separate feed−back networks (see Figure 11):

- One for regulation applied to pin 4 (feed−back input).
- Another one for the OVP function.

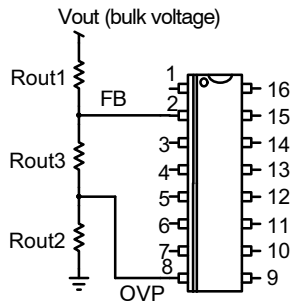


Figure 10. Configuration with One Feed−back Network for Both OVP and Regulation

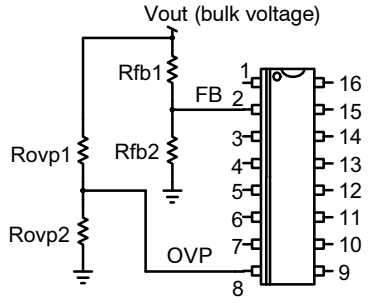


Figure 11. Configuration with Two Separate Feed−back Networks

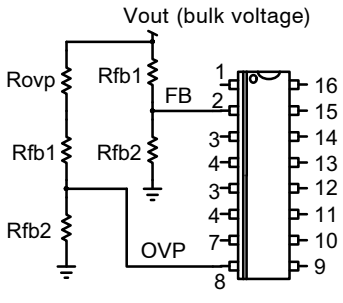


Figure 12. Another Configuration with Two Separate Feed−back Networks

The double feed−back configuration offers some redundancy and hence, an up−graded safety level as it protects the PFC stage even if there is a failure of one of the two feed−back arrangements.

However, the regulation and the OVP function have the same reference voltage (V_{REF} = 2.5 V) so that if wished, one single feed−back arrangement is possible as portrayed by Figure 9. The regulation and OVP blocks having the same reference voltage, the resistance ratio $R_{out}2$ over $R_{out}3$ adjusts the OVP threshold. More specifically,

- The bulk regulation voltage is:

$$V_{out,nom} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2} + R_{out3}} \cdot V_{REF} \quad \text{(eq. 84)}$$

- The (bulk) OVP level is:

$$V_{out,ovp} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2}} \cdot V_{REF} \quad \text{(eq. 85)}$$

- The ratio OVP level over regulation level is:

$$\frac{V_{out,ovp}}{V_{out,nom}} = 1 + \frac{R_{out3}}{R_{out2}} \quad \text{(eq. 86)}$$

For instance, (R_{out3} = 5% x R_{out2}) leads to ($V_{out,ovp}$ = 105% x $V_{out,nom}$).

As soon and as long as the circuit detects that the output voltage exceeds the OVP level, the power switch is turned off to stop the power delivery.

In our application, the option that consists of two separate V_{out} sensing networks is chosen (configuration of Figure 10). Like for the regulation network, the impedance of the monitoring resistors must be:

1. high enough to limit the losses that if excessive, may not allow to comply with the stand−by requirements to be met by most power supplies
2. low enough for a good noise immunity

Again, a bias current in the range of 100 μA generally gives a good trade−off.

$$\text{Hence:} \qquad R_{ovp2} = \frac{V_{ref}}{100\ \mu A} = 25\ k\Omega \qquad \text{(eq. 87)}$$

In practice, (R_{ovp2} = 27 kΩ) was selected and as a consequence:

$$R_{ovp1} = R_{ovp2} \cdot \left(\frac{V_{out,ovp}}{V_{REF}} - 1 \right) \qquad \text{(eq. 88)}$$

In our application, our 410−V target leads to:

$$R_{ovp1} = 27\ k\Omega \cdot \left(\frac{410}{2.5} - 1 \right) = 4401\ k\Omega \qquad \text{(eq. 89)}$$

For safety reason, several resistors should be placed in series instead of a single R_{ovp1} one. In our application, we choose a (1800 kΩ + 1800 kΩ + 820 kΩ) network.

The exact OVP level is then:

$$V_{out,ovp} = \frac{R_{ovp1} + R_{ovp2}}{R_{ovp2}} \cdot V_{REF} = \frac{1800\ k + 1800\ k + 820\ k + 27\ k}{27\ k} \cdot 2.5\ V \cong 412\ V \qquad \text{(eq. 90)}$$

Remark:

As illustrated by Figure 11, another effective means to dimension the OVP sensing network is, to select:

- $R_{ovp2} = R_{fb2}$
- $R_{ovp1} = R_{fb1} + R_{ovp}$, where R_{ovp} is a part of the upper resistor of the OVP sensing network.

Note that:

$$V_{out,nom} = \frac{R_{fb1} + R_{fb2}}{R_{fb2}} \cdot V_{REF}$$

$$V_{out,ovp} = \frac{R_{ovp1} + R_{ovp2}}{R_{ovp2}} \cdot V_{REF} = \frac{R_{fb1} + R_{ovp} + R_{fb2}}{R_{fb2}} \cdot V_{REF}$$

Combining two precedent equations, it comes:

$$V_{out,ovp} = V_{out,nom} + \frac{R_{ovp}}{R_{fb2}} \cdot V_{REF}$$

In other words, the OVP protection trips when the overshoot exceeds:

$$\left(\frac{R_{ovp}}{R_{fb2}} \cdot V_{REF} \right)$$

Conclusions

This application note proposes a systematic approach for the eased design of an efficient 2−phase, interleaved PFC. More specifically, this paper provides the key equations and design criteria necessary to dimension the PFC stage. The practical implementation of a 300−W, wide mains application illustrates the process.

For detailed information on the performance of a 300−W interleaved PFC designed according to the proposed method, you can refer to NCP1631EVB/D [3]. This application note shows that the efficiency can remain as high as almost 95% at 90 V_{rms} from 20% to 100% of the load, despite the relatively high switching frequency range that was selected (120−kHz nominal clamp frequency).

The following table summarizes the key equations useful to design a NCP1631 driven interleaved PFC. Another table reports the results of these computations for our 300−W application of interest.

References

[1] Joel Turchi, “Characteristics of Interleaved PFC Stages”, Application Note AND8355, http://www.onsemi.com/pub/Collateral/AND8355−D.PDF

[2] Joel Turchi, “Designing a high−efficiency, 300−W, wide mains interleaved PFC”, Application Note AND8354, http://www.onsemi.com/pub/Collateral/AND8354−D.PDF

[3] Stephanie Conseil, “Performance of a 300−W, wide mains interleaved PFC driven by the NCP1631”, NCP1631EVB/D, http://www.onsemi.com/pub/Collateral/NCP1631EVB−D.PDF

Table 1. GENERAL EQUATIONS − SUMMARY

Power Components	Coil Selection	$L \geq \frac{(V_{in,rms})_{LL}^{\,2} \cdot \left(V_{out,nom} - \sqrt{2} \cdot (V_{in,rms})_{LL}\right)}{(P_{in,avg})_{max} \cdot V_{out,nom} \cdot f_{OSC(nom)}}$ $(I_{L,pk})_{max} = \sqrt{2} \cdot \frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}}$ $(I_{L,rms})_{max} = \frac{1}{\sqrt{3}} \cdot \frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}}$
	MOSFET Conduction Losses	$(P_{on})_{max} = \frac{1}{3} \cdot R_{DS(on)} \cdot \left(\frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}}\right)^2 \cdot \left[1 - \frac{8\sqrt{2} \cdot (V_{in,rms})_{LL}}{3\pi \cdot V_{out,nom}}\right]$
	Bulk Capacitor	$(\delta V_{out})_{pk-pk} = \frac{P_{out,max}}{C_{bulk} \cdot \omega \cdot V_{out,nom}}$ $C_{bulk} \geq \frac{2 \cdot P_{out,max} \cdot t_{HOLD-UP}}{V_{out,nom}^{\,2} - V_{out,min}^{\,2}}$ $(I_{C,rms})_{max} = \sqrt{\left(\frac{16\sqrt{2}}{9\pi} \cdot \frac{(P_{in,avg})_{max}^{\,2}}{(V_{in,rms})_{LL} \cdot V_{out,nom}}\right) - \left(\frac{(P_{out})_{max}}{V_{out,nom}}\right)^2}$
Brown−out Block	BO Upper Resistor	$R_{bo1} = \frac{(V_{in,avg})_{boH} - \left((V_{in,avg})_{boL} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)\right)}{I_{HYST}}$
	BO Bottom Resistor	$R_{bo2} = \frac{R_{bo1}}{\left(\frac{(V_{in,avg})_{boL}}{V_{BO(th)}} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)\right) - 1}$
	BO Filtering Capacitor	$C_{bo} = \frac{R_{bo1} + R_{bo2}}{2\pi \cdot R_{bo1} \cdot R_{bo2} \cdot f_{BO}}$
Timing Resistor	Pin3 Resistor	$R_t = 4026 \cdot 10^3 \cdot k_{BO} \cdot \sqrt{L \cdot (P_{in})_{HL}}$
Oscillator	Oscillator Frequency (No Frequency Foldback)	$f_{OSC(nom)} \cong \frac{52 \cdot 10^{-6}}{C_{OSC}}$
	Clamp Frequency per Branch	$\left(f_{sw(max)}\right)_{nom} = \frac{f_{OSC(nom)}}{2} \cong \frac{26 \cdot 10^{-6}}{C_{OSC}}$
	Fold−Forward Power Threshold	$(P_{in})_{FF} = \frac{R_{FF}}{15810\ \Omega} \cdot (P_{in})_{HL}$
	Minimum Frequency (per Branch)	$\left(f_{sw(max)}\right)_{min} = \frac{1}{2 \cdot R_{Fmin} \cdot C_{OSC} \cdot \left(0.22 + \ln\left(\frac{R_{Fmin} - 114000}{R_{Fmin} - 143000}\right)\right)}$

Table 1. GENERAL EQUATIONS – SUMMARY

Feedback Resistors	Feedback Bottom Resistor	$R_{fb2} = \frac{V_{REF}}{I_{FB}}$
	Feedback Upper Resistor	$R_{fb1} = R_{fb2} \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1 \right)$
OVP Resistors	OVP Bottom Resistor	$R_{ovp2} = \frac{V_{REF}}{I_{FB}}$
	OVP Upper Resistor	$R_{ovp1} = R_{ovp2} \cdot \left(\frac{V_{out,ovp}}{V_{REF}} - 1 \right)$
Loop Compensation	C_p Capacitor of the Type2 Compensation	$C_p \cong \frac{1.06 \cdot 10^{-6} \cdot (P_{in})_{HL}}{C_{bulk} \cdot {f_c}^2 \cdot (V_{out,nom})^2}$
	C_z Capacitor of the Type2 Compensation	$C_z = 15 \cdot C_p$
	R_z Resistor of the Type2 Compensation	$R_z = \frac{2}{\pi \cdot C_z \cdot f_c}$
Current Limitation	Maximum Level of the Input Current	$I_{in,max} = 2\sqrt{2} \cdot \frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}} \cdot \left[1 - \frac{V_{out,nom}}{4 \cdot \left(V_{out,nom} - \left(\sqrt{2} \cdot (V_{in,rms})_{LL} \right) \right)} \right]$ if $(V_{in,rms})_{LL} \le \frac{V_{out,nom}}{2\sqrt{2}}$ $I_{in,max} = 2\sqrt{2} \cdot \frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}} \cdot \left(1 - \frac{V_{out,nom}}{4 \cdot \sqrt{2} \cdot (V_{in,rms})_{LL}} \right)$ if $(V_{in,rms})_{LL} \ge \frac{V_{out,nom}}{2\sqrt{2}}$
	Current Sense Resistor	$R_{CS} = \frac{P_{Rcs} \cdot {(V_{in,rms})_{LL}}^2}{{(P_{in,avg})_{max}}^2}$
	Over Current Resistor	$R_{OCP} = \frac{R_{CS} \cdot I_{in,max}}{210 \cdot 10^{-6}}$

- $f_{OSC(nom)}$ is the oscillator frequency without frequency foldback
- ($f_{sw(max)}$) is the nominal clamp frequency for each branch (in the absence of frequency foldback), that is $\left(\frac{f_{OSC(nom)}}{2}\right)$
- $(f_{sw(max)})_{min}$ is the minimum clamp frequency for each branch resulting from frequency foldback
- $V_{out,nom}$ is the nominal output voltage of the PFC stage (regulation level)
- $(V_{in,rms})_{LL}$ is the lowest level of the line rms voltage
- $(P_{in,avg})_{max}$ is the maximum level of the average input power
- $(I_{L,pk})_{max}$ is the maximum peak current absorbed by one branch of the interleaved PFC (normal operation)
- $(I_{L,rms})_{max}$ is the maximum rms current drawn by one branch of the interleaved PFC (normal operation)
- P_{on} are the MOSFET conduction losses (in one branch)
- $R_{DS(on)}$ is the MOSFET on−time resistor (for one branch)
- $(\delta V_{out})_{pk-pk}$ is the output peak to peak ripple
- ω is the line angular frequency ($\omega = 2\pi \times f_{line}$)
- f_{line} is the line frequency
- C_{bulk} is the bulk capacitor
- $t_{HOLD-UP}$ is the specified hold−up time
- $(I_{C,rms})_{max}$ is the rms current of the bulk capacitor. Its given computation assumes a resistive load.
- $V_{out,min}$ is the minimum level of the output voltage that is acceptable for the downstream converter
- $(P_{in})_{HL}$ is the maximum level that can be virtually delivered by the PFC stage as allowed by the timing resistor selection. For the sake of a welcome margin, ($(P_{in})_{HL}$) should be selected about 30% higher than the expected maximal input power that is:
  $\left((P_{in})_{HL} = 130\% \cdot (P_{in,avg})_{max}\right)$
- $(P_{in})_{FF}$ is the input power level below which the circuit starts to reduce the switching frequency (Frequency Fold−back)
- R_{FF} is the resistor to be placed between pin6 and ground to control the frequency fold−back characteristic
- R_{Fmin} is the resistor that can be placed between the oscillator pin and ground to adjust a minimum frequency. The moderate impact on the $f_{OSC(nom)}$ value is not taken into account in the given $f_{OSC(nom)}$ computation equation.
- R_{fb1} and R_{fb2} are the feedback sensing resistors.
- R_{ovp1} and R_{ovp2} are the OVP sensing resistors.
- $V_{out,ovp}$ is the OVP output voltage.
- V_{REF} is the internal 2.5−V voltage reference.
- R_{bo1} and R_{bo2} are the Brown−Out sensing resistors.
- k_{BO} is the brown−out scaling down factor
  $\left(k_{BO} = \frac{R_{bo2}}{R_{bo1} + R_{bo2}}\right)$
- f_{BO} is the frequency pole created by the BO pin external capacitor (C_{bo}) together with R_{bo1} and R_{bo2}
- I_{HYST} is the internal 7−μA internal current source used for hysteresis
- $(V_{in,avg})_{boH}$ is the averaged input voltage at which the circuit starts operation.
  $\left((V_{in,avg})_{boH} = \sqrt{2} \cdot V_{in,rms}\right)$ in a traditional PFC stage.
- $(V_{in,avg})_{boL}$ is the averaged input voltage below which the Brown−out protection trips.
  $\left((V_{in,avg})_{boH} = \frac{2\sqrt{2}}{\pi} \cdot V_{in,rms}\right)$ in a traditional PFC stage.
- $V_{BO(th)}$ is the internal 1−V brown−out voltage reference.
- R_z, C_z and C_p are the compensation components.
- f_c is the crossover frequency.
- R_{CS} is the current sense resistor.
- P_{Rcs} are the losses across R_{sense}. 0.2% of the maximum power generally gives a good trade−off between noise immunity and efficiency.
- R_{OCP} is the resistor that placed between the CS pin and R_{CS}, sets the maximum level of the input current (total current absorbed by the two branches).

Remark Regarding the Compensation:

The compensation is computed to have a phase margin in the range of 60°. The high frequency pole can be set at a lower frequency. Practically, C_p can be increased up to 4 times the proposed value (without changing $\boldsymbol{R_z}$ and $\boldsymbol{C_z}$) to reduce the ripple on the $\boldsymbol{V_{control}}$ pin and further improve the THD. This is at the cost of a diminution of the phase margin that can drop as low as 30°.

Example 1: 300−W, Wide Mains Application

We select a 120−kHz frequency clamp per branch.

The maximum output power being 300 W, we estimate that the input power can be as high as around 325 W (92% efficiency at the lowest line – conservative figure that offers some margin). The power capability ($(P_{in})_{HL}$) is set 125% higher at 400 W.

The minimum input voltage being 90 V_{rms}, the brown−out block is dimensioned so that the circuit starts operating when the line rms voltage exceeds 81 V and a brown−out fault is detected when the line magnitude goes below 72 V.

The regulation level is set to 390 V ($V_{out,nom}$ = 390 V) and the OVP level to 410 V ($V_{out,ovp}$ = 410 V).

A 100−μF bulk capacitor is implemented.

The current resistor is selected so that it does not consume more than about 0.2% of the maximum power (P_{Rsense} = 0.2% x $(P_{in,avg})_{max}$).

Table 2.

Power Components	Coil Selection	$L \geq \frac{90^2 \cdot \left(390 - \sqrt{2} \cdot 90\right)}{320 \cdot 390 \cdot 120\,k} \cong 140\ \mu H$ $(I_{L,pk})_{max} = \sqrt{2} \cdot \frac{320}{90} \cong 5.0\ A$ $(I_{L,rms})_{max} = \frac{1}{\sqrt{3}} \cdot \frac{320}{90} \cong 2.1\ A$ A 150−μH / 6 Apk / 2.5 A_{rms} coil was selected
	MOSFET Conduction Losses	$(P_{on})_{max} = \frac{1}{3} \cdot R_{DS(on)} \cdot \left(\frac{320}{90}\right)^2 \cdot \left[1 - \frac{8\sqrt{2} \cdot 90}{3\pi \cdot 390}\right] \cong 3 \cdot R_{DS(on)}$
	Bulk Capacitor	$(\delta V_{out})_{pk-pk} = \frac{300}{100\ \mu \cdot 2\pi \cdot 60 \cdot 390} \cong 20\ V \quad (f_{line} = 60\ Hz)$ $C_{bulk} \geq \frac{2 \cdot 300 \cdot t_{HOLD-UP}}{390^2 - 330^2} \cong 0.014 \cdot t_{HOLD-UP}$ $(I_{C,rms})_{max} = \sqrt{\left(\frac{16\sqrt{2}}{9\pi} \cdot \frac{325^2}{90 \cdot 390}\right) - \left(\frac{300}{390}\right)^2} \cong 1.3\ A$
Brown−out Block	BO Upper Resistor	$R_{bo1} = \frac{115 - \left(65 \cdot \left(1 - \frac{10\%}{3}\right)\right)}{7 \cdot 10^{-6}} \cong 7450\ k\Omega \Rightarrow 7200\ k\Omega$
	BO Bottom Resistor	$R_{bo2} = \frac{7200 \cdot 10^3}{\left(\frac{65}{1} \cdot \left(1 - \frac{10\%}{3}\right)\right) - 1} \cong 116\ k\Omega \Rightarrow 120\ k\Omega$
	BO Filtering Capacitor	$C_{bo} = \frac{7200\,k + 120\,k}{2\pi \cdot 7200\,k \cdot 120\,k \cdot 10\% \cdot f_{line}} \cong \frac{13.5 \cdot 10^{-6}}{f_{line}} \cong 220\ nF$ $(f_{line} = 60\ Hz)$
Timing Resistor	Pin3 Resistor	$R_t = 4026 \cdot 10^3 \cdot \frac{120\,k}{7200\,k + 120\,k} \cdot \sqrt{150\ \mu \cdot 400} \cong 16.2\ k\Omega \Rightarrow 18\ k\Omega$ $\Rightarrow (P_{in})_{HL} = 494\ W$
Oscillator	Oscillator Frequency (No Frequency Foldback)	$f_{OSC(nom)} \cong \frac{52 \cdot 10^{-6}}{220 \cdot 10^{-12}} \cong 236\ kHz$
	Clamp Frequency per Branch	$\left(f_{sw(max)}\right)_{nom} = \frac{f_{OSC(nom)}}{2} \cong 118\ kHz$
	Fold−Forward Power Threshold	$(P_{in})_{FF} = \frac{R_{FF}}{15810\ \Omega} \cdot (P_{in})_{HL} = \frac{4700\ \Omega}{15810\ \Omega} \cdot 494 \cong 147\ W$
	Minimum Frequency (per Branch)	$\left(f_{sw(max)}\right)_{min} = \frac{1}{2 \cdot 270\,k \cdot 220\,p \cdot \left(0.22 + \ln\left(\frac{270\,k - 114\,k}{270\,k - 143\,k}\right)\right)} \cong 19.8\ kHz$
Feedback Resistors	Feedback Bottom Resistor	$R_{fb2} = \frac{2.5}{92\ \mu} \cong 27\ k\Omega$
	Feedback Upper Resistor	$R_{fb1} = 27\,k \cdot \left(\frac{390}{2.5} - 1\right) = 4185\ k\Omega$
OVP Resistors	OVP Bottom Resistor	$R_{ovp2} = \frac{2.5}{92\ \mu} \cong 27\ k\Omega$
	OVP Upper Resistor	$R_{ovp1} = 27\,k \cdot \left(\frac{410}{2.5} - 1\right) \cong 4400\ k\Omega$

Table 2.

Loop Compensation	C_p Capacitor of the Type2 Compensation	$C_p \cong \frac{1.06 \cdot 10^{-6} \cdot 494}{100 \cdot 10^{-6} \cdot 20^2 \cdot 390^2} \cong 86\ nF$ $\Rightarrow 68\ nF$
	C_z Capacitor of the Type2 Compensation	$C_z = 15 \cdot 68\ n \cong 1.02\ \mu F$ $\Rightarrow 1.0\ \mu F$
	R_z Resistor of the Type2 Compensation	$R_z = \frac{2}{\pi \cdot 1.0\ \mu \cdot 20} \cong 31.8\ k\Omega$ $\Rightarrow 33\ k\Omega$
Current Limitation	Maximum Level of the Input Current	$I_{in,max} = 2\sqrt{2} \cdot \frac{325}{90} \cdot \left[1 - \frac{390}{4 \cdot \left(390 - \left(\sqrt{2} \cdot 90\right)\right)}\right] \cong 6.4\ A$
	Current Sense Resistor	$R_{CS} = \frac{0.2\% \cdot 325 \cdot 90^2}{325^2} = 49.8\ m\Omega$ $\Rightarrow 50\ m\Omega$
	Over Current Resistor	$R_{OCP} = \frac{50 \cdot 10^{-3} \cdot 6.4}{210 \cdot 10^{-6}} \cong 1.52\ k\Omega$ $\Rightarrow 1.5\ k\Omega$

BILL OF MATERIALS

Table 3. BILL OF MATERIALS*

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed
CM1	1	CM Filter, 4 A	2*6.8 mH	4 A / 250 V	through-hole	EPCOS	B82725-A2402-N1	NO
C2	1	Electrolytic capacitor	100 μF	450 V	through-hole	BC Components	2.22216E+11	NO
C5	1	X2 capacitor	100 nF	275 V	through-hole	RIFA	PHE840MB6100MB05R17	NO
C6	1	X2 capacitor	1 μF	275 V	through-hole	RIFA	PHE840MD7100MD20R06L2	NO
C10, C16	2	Y capacitor	4.7 nF	275 V	through-hole	Murata	DE1E3KX472MA5B	NO
C15	1	Ceramic capacitor	220 pF	5%, 50 V	SMD, 1206			YES
C18	1	X2 capacitor	680 nF	275 V	through-hole	EPCOS	B32923A2684M	NO
C20	1	Ceramic capacitor	150 nF	10%, 50 V	SMD, 1206			YES
C22, C27	2	Ceramic capacitor	1 nF	10%, 50 V	SMD, 1206			YES
C25	1	Ceramic capacitor	1 μF	10%, 50 V	SMD, 1206			YES
C28	1	Ceramic capacitor	220 nF	10%, 50 V	SMD, 1206			YES
C30, C33	2	Ceramic capacitor	100 nF	10%, 50 V	SMD, 1206			YES
C32	1	Electrolytic capacitor	100 uF	25 V	through-hole			YES
C34	1	Ceramic capacitor	10 nF	10%, 50 V	SMD, 1206			YES
D6, D14, D15	3	Diode	D1N4148		through-hole	Philips	1N4148	YES
D3	1	LED 3mm	2.4V/2mA		through-hole	Vishay	TLLG4400	YES
D4, D5	2	Boost diode	MUR550	5 A, 500 V	Axial	ON Semiconductor	MUR550APFG	NO
D16	1	Standard recovery diode, 600 V	1N5406	3 A, 600 V	Axial	ON Semiconductor	1N5406G	NO
D21	1	Zener diode, 18 V	18 V		through-hole	NXP	BZX79-C18	NO

*All products listed are Pb−free.

Table 3. BILL OF MATERIALS*

Desig-nator	Qty	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number	Substi-tution Allowed
HS1	1	Heatsink, 2.9 °C/W	2.9 °C/W			AAVID THERMALLOY	437479	NO
L4	1	DM Choke, WI-FI series	150 μH/ 5 A	20%, 5 A	through-hole	Wurth Electronics	7447076	NO
Q1, Q2	2	PNP transistor	2N2907		TO92	ON Semiconductor	MPS2907AG	NO
R2, R6	2	Axial resistor, 1/4 W	1 kW	1%	through-hole			YES
R1	1	Axial resistor, 1/4 W	1.8 kW	1%	through-hole			YES
R7, R17	2	Axial resistor, 1/4 W	2.2 W	1%	through-hole			YES
R11, R20	3	SMD resistor, 1206, 1/4 W	10 kW	1%	SMD, 1206			YES
R14, R15	2	SMD resistor, 1206, 1/4 W	22 kW	1%	SMD, 1206			YES
R16, R21	2	Axial resistor, 1/4 W	0 W	1%	through-hole			YES
R18	1	Axial resistor, 1/4 W	560 kW	0.01	through-hole			YES
R23	1	Axial resistor, 1/4 W	820 kW	0.01	through-hole			YES
R24	1	Axial resistor, 3 W, ±1%	50 mW	0.01	through-hole	Vishay	RLP3 0R050	NO
R25, R40	2	SMD resistor, 1206, 1/4 W	27 kW	0.01	SMD, 1206			YES
R31, R32, R38, R39, R41, R42, R43, R44	8	Axial resistor, 1/4 W	1800 kW	1%, 1/4 W	through-hole			YES
R33	1	SMD resistor, 1206, 1/4 W	18 kW	0.01	SMD, 1206			YES
R34	1	SMD resistor, 1206, 1/4 W	270 kW	0.01	SMD, 1206			YES
R36	1	SMD resistor, 1206, 1/4 W	33 kW	0.01	SMD, 1206			YES
R37	1	SMD resistor, 1206, 1/4 W	4.7 kW	0.01	SMD, 1206			YES
R45	1	SMD resistor, 1206, 1/4 W	0 W	0.01	SMD, 1206			YES
R46	1	SMD resistor, 1206, 1/4 W	120 kW	0.01	SMD, 1206			YES
R121, R122, R123	3	SMD resistor, 1206, 1/4 W	680 kW	0.01	SMD, 1206			YES
U1	1	Diode Bridge	KBU6K			General Semiconductor	KBU6K	NO
U2	1	Interleaved PFC controller, SOIC-16	NCP1631	-	SO16	ON Semiconductor	NCP1631	NO
X1, X5	2	PFC coil	150 μH	-		CME	OF9120	NO
X4, X6	2	MOSFET	IPP50N250 CP	550 V	TO220	Infineon	IPP50N250CP	NO
	2	TO220 isolators				Bergquist	3223-07FR-43	YES
	5	Board “legs”				RICHCO	TCBS-801	YES
F1	1	Fuse	4A Temporised	250 V		Shurter	34.3123	YES
X4, X6	2	MOSFET	IPP50N250 CP	550 V	TO220	Infineon	IPP50N250CP	NO
VOUT	1	Connector	-	-	-	Multi Contact	23.3200-22	YES
GND	1	Connector	-	-	-	Multi Contact	23.3200-21	YES
J1	1	Connector	-	-	-	Schurter	GSF1.1201.31	YES
J2	1	Connector	-	-	-	Weidmuller	PM 5.08/2/90 3.5 SW	YES

*All products listed are Pb−free.

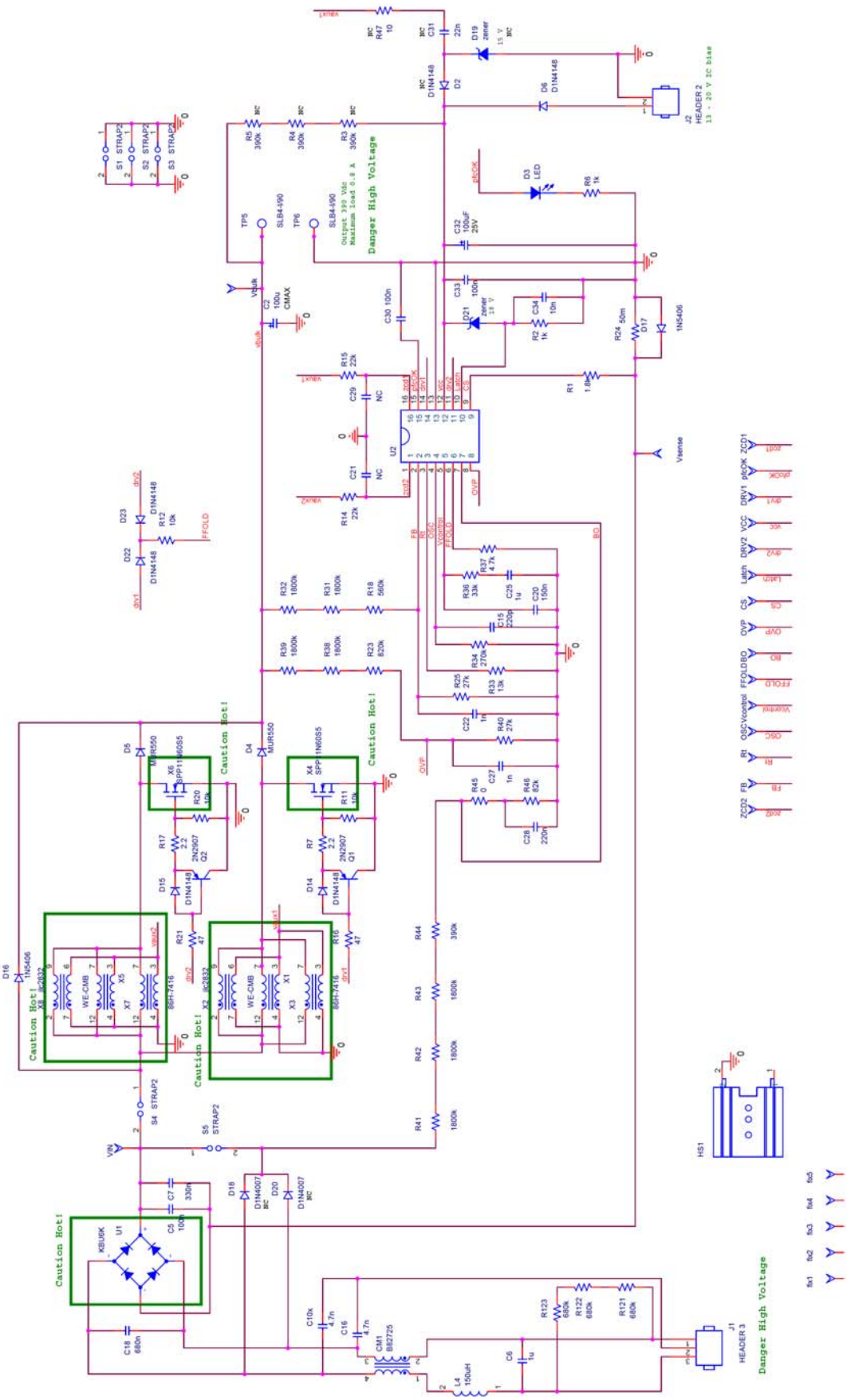


Figure 13. Evaluation Board Schematic

TEST PROCEDURE FOR THE NCP1631PFCGEVB EVALUATION BOARD

- **The board contains high voltage, hot, live parts.**
- **Be very cautious when manipulating or testing it.**
- **It is the responsibility of those who utilize the board, to take all the precautions to avoid that themselves or other people are injured by electric hazards or are victim of any other pains caused by the board.**
- Input Range: 85 to 265 Vrms.
- Output Voltage: 390 Vdc
- Output Power Range: 0 to 300 W
- Brown-out levels:
  - Starts operation when the line voltage exceeds about 84 Vrms.
  - Stops operation when the line voltage drops below 72 Vrms.
- The NCP1631 is to be supplied by an external power source ranging from 13 V to 20 Vdc.
- The board PCB offers the option where NCP1631 is self-supplied. For that, some components are to be added (see relevant application note).

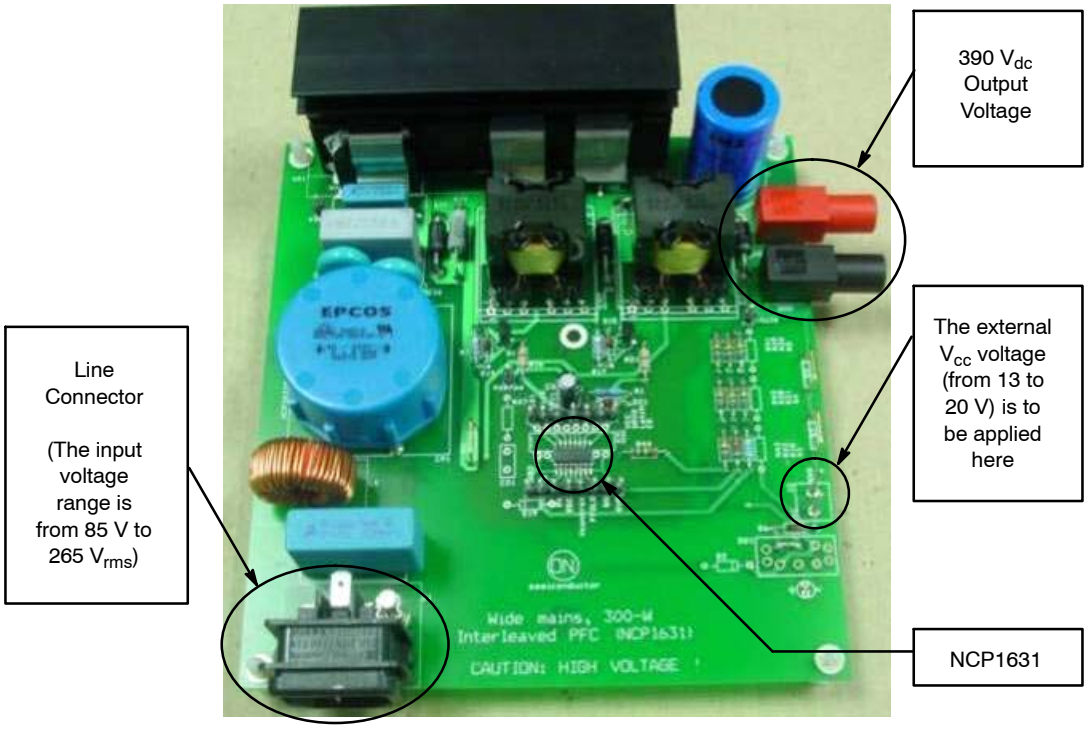


Figure 14. NCP1631GEVB Evaluation Board

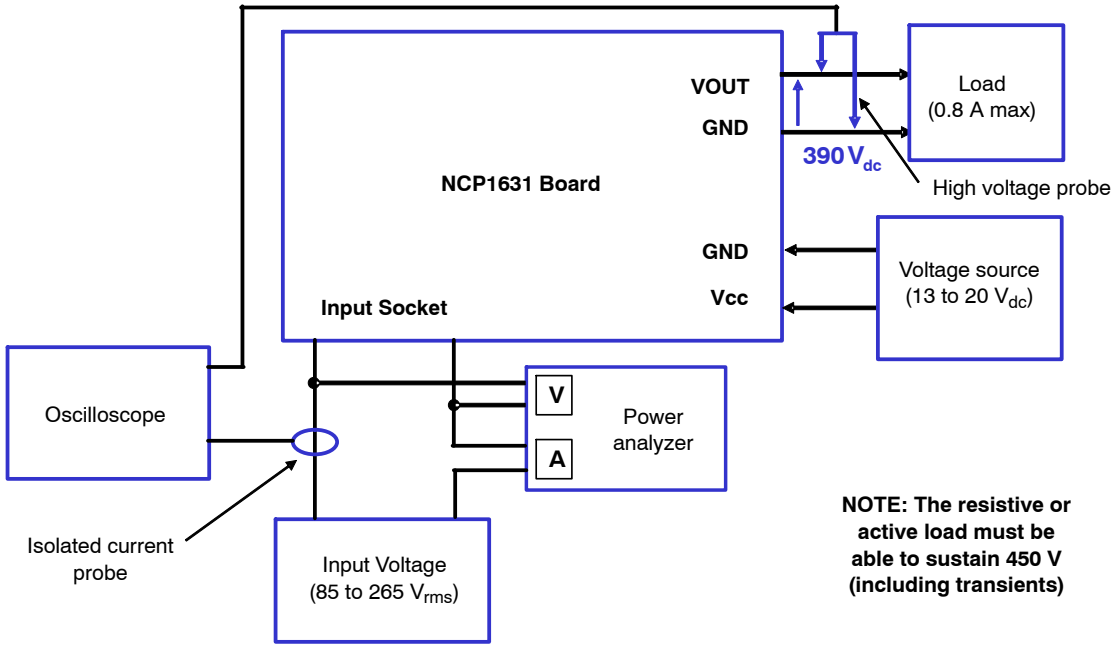


Figure 15. Test Setup

Test 1

1. Apply the input voltage 115 Vrms to the input socket.
2. Connect a load between the (Vout;GND) terminals. Set the output current (Iout) to 0.8 A.
3. Place a power analyser able to measure: the input power (Pin),the power factor (PF), the total harmonic distorsion (THD)
4. Apply the VCC voltage 15 Vdc.
5. Verify that:

Parameters	Comments	Limits
V_{OUT}	Voltage measured between "V_{OUT}" and "GND"	370 V < V_{OUT} < 409 V
PF	Power Factor	> 0.980
THD	Total Harmonic Distortion	< 13 %
Efficiency	$V_{out}I_{out}$ / P_{in}	> 96 %

Test 2

6. Observe the input current using an oscilloscope and a current probe. The current is nearly sinusoidal.
7. Increase the input voltage to 230 Vrms
8. Verify that:

Parameters	Comments	Limits
V_{OUT}	Voltage measured between "V_{OUT}" and "GND"	370 V < V_{OUT} < 409 V
PF	Power Factor	> 0.970
THD	Total Harmonic Distortion	< 13 %
Efficiency	$V_{out}I_{out}$ / P_{in}	> 97.5 %

Test 3: OCP

9. Set the input voltage to 90 Vrms and the output current to 0.8 A.
10. Gradually decrease the input voltage while observing the input current with the oscilloscope until the top of the sinusoid becomes flat as in the blue curve in Figure 16.
11. Measure the plateau: it must be between 7.27 and 8.13 A

Test 4: OVP

12. Observe the output voltage with an oscilloscope. Set the triggering level at about 200 V, the trigger position being set at 10% of the screen. Program the scope to observe 50 or 100 ms in single acquisition mode.
13. Set the input voltage to 115 Vrms and apply it to the board.
14. Abruptly apply the VCC voltage (15 V). Check that the output voltage keeps below 424 V.

Test 5: Frequency Foldback

15. Set the output current to 0.07 A and the input voltage to 115 Vrms.
16. Connect a voltage probe to the test point DRV1 on the board and a current probe to observe the input current.
17. Set the trigger at the top of input current sinusoid and zoom in to see the DRV pulses.
18. Measure the switching frequency: it should be between 35 kHz and 50 kHz.

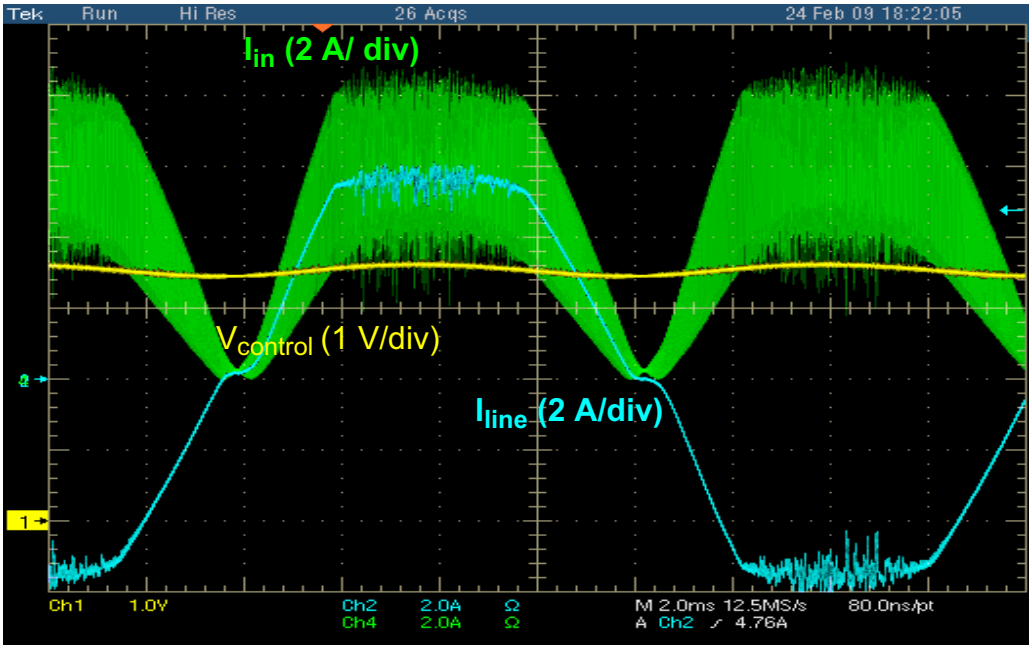


Figure 16.

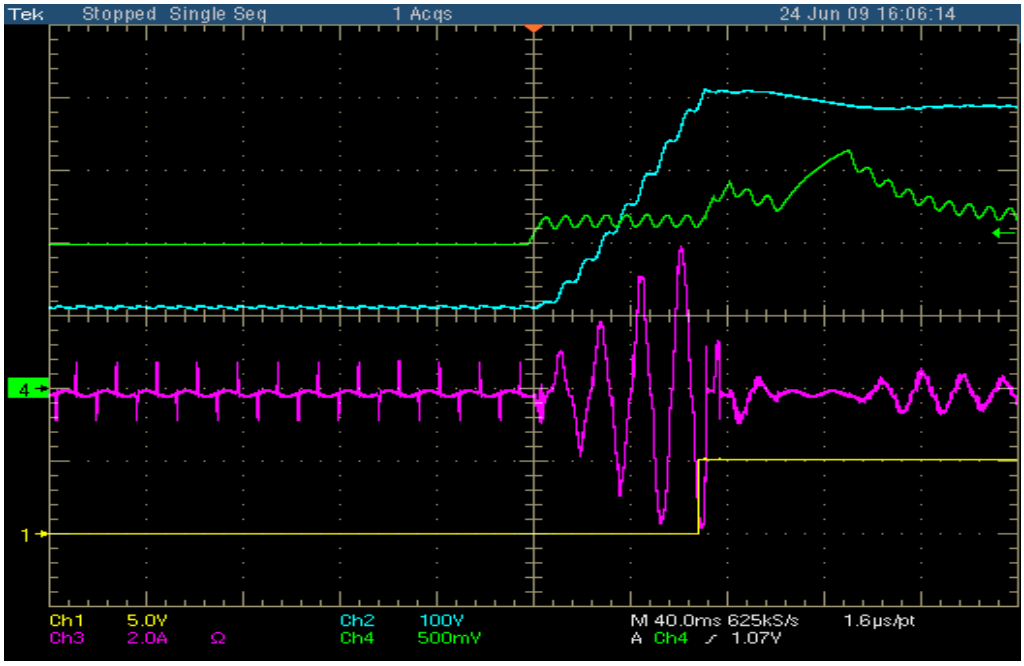


Figure 17.

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